PROJECT N10I

Revision 2008/04/24

Revision History

R1.0	S R	2008/01

Power States

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+*VALWAYSP	+*V	+*VS	Clocks
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5/Soft OFF	LOW	LOW	LOW	ON	OFF	OFF	OFF

S M B S i g n a l s

Host	Name	Devices	Address
Chipset	SMBCK,SMBDA	ICH7-M ADT7473(Thermal) ICS954310(Clock Genertor) DDR2 SO-DIMM	0001 000X b 0101 110X b D2h A0h

P C I D e v i c e s

Bus#	Device#	Function#	REQ/GNT#	IDSEL	APIC Interrupts	Device Function
Bus0	Device00	Function0				Intel 945GMS Host Bridge
Bus0	Device02	Function0				VGA-Comptible Controller
Bus0	Device1C	Function0				PCI to PCI Bridge
Bus0	Device27	Function0			A#	Azalia Controller
Bus0	Device29	Function0			H#	Intel UHCI USB Cotroller
Bus0	Device29	Function1			D#	Intel UHCI USB Cotroller
Bus0	Device29	Function2			C#	Intel UHCI USB Cotroller
Bus0	Device29	Function3			A#	Intel UHCI USB Cotroller
Bus0	Device29	Function7			H#	Intel EHCI USB Cotroller
Bus0	Device31	Function1			C#	PATA
Bus0	Device31	Function2			B#	SATA
Bus5	Device08	Function0		AD17	B#	CarBus Brige

V o l t a g e R a i l

Net Name	Voltage	On During These ACPI States	Description
+3VAO,+3VA,+3VALWAYS_P	+3.3V	S0 - S5	Always ON.
+5VCHG	+5V		
+VCC_RTC	+5V		
+3VO,+3VSUS,+3VALWAYS	+3V	S0,S3,S4*,S5*	Power supply for ICH7M, RTL8111B.
+5VO,+5VSUS	+5V		
+1.8VO,+1.8V	+1.8V	S0 - S3	Power supply for 945GMS,DDRII,ICH7M,M38857 R5C801.
+3V	+3V		
+5V	+5V		
+1.05VO,+VCCP	+1.05V	S0	0.9V DDR2 termination voltage
+1.5VO,+1.5VS	+1.5V		Core voltage for processor
+0.9VO,+0.9VS	+0.9V		
+2.5VO,+2.5VS,VCCA3GBG	+2.5VS		
VCCALVDS,VCCSYNC,VCCTXLVDS			
+3VS	+3V		
+5VS	+5V		
+VCORE_O,+VCORE	Variable		

ASUS	Title : Table of Contens	
ASUSTeK COMPUTER INC	Engineer: ENGINEER	
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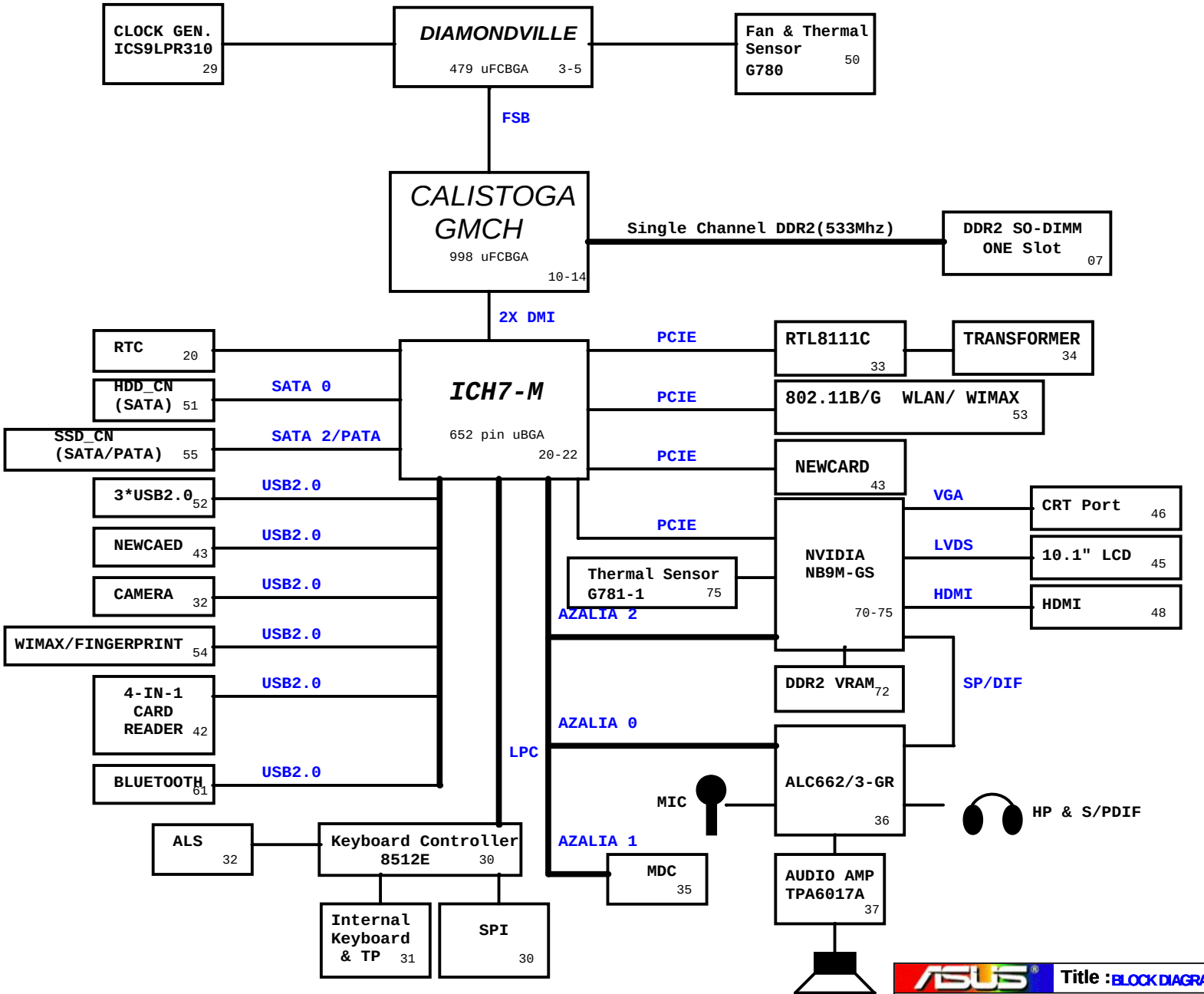
DIAMONDVILLE/CALISTOGA(945GSE) BLOCK DIAGRAM



POWER

VCORE	80
SYSTEM	81
VCCP, +1.5VS	82
+1.8V, +0.9VS	83
+2.5VS, +3VA	84
+VGA_CORE, +1.1VS	85
EMPTY	86
EMPTY	87
CHARGER	88
EMPTY	89
POWER PROTECT	90
LOAD SWITCH	91
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ASUSTeK COMPUTER INC

Title : BLOCK DIAGRAM

Engineer: ENGINEER

Size	Project Name	Rev
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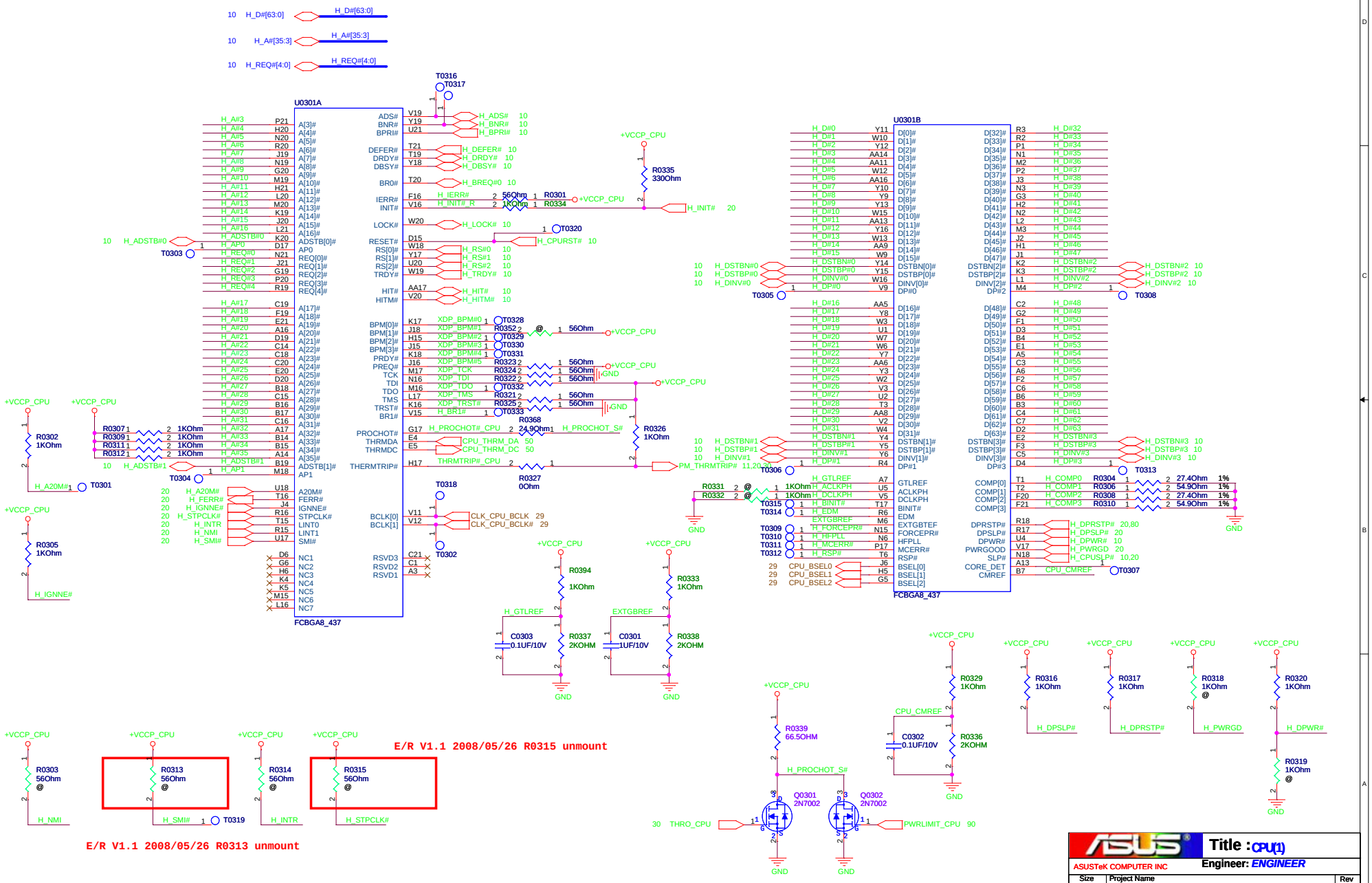
U0301A
FCBGA8_437
U0301B
FCBGA8_437
H_D#[63:0]
H_A#[35:3]
H_REQ#[4:0]
H_ADSTB#0
H_ADSTB#1
H_DSTBN#0
H_DSTBP#0
H_DINV#0
H_DSTBN#1
H_DSTBP#1
H_DINV#1
H_DSTBN#2
H_DSTBP#2
H_DINV#2
H_DSTBN#3
H_DSTBP#3
H_DINV#3
H_ADS#
H_BNR#
H_BPRI#
H_DEFER#
H_DRDY#
H_DBSY#
H_BREQ#0
H_IERR#
H_INIT#_R
H_INIT#
H_LOCK#
H_CPURST#
H_RS#0
H_RS#1
H_RS#2
H_TRDY#
H_HIT#
H_HITM#
XDP_BPM#0
XDP_BPM#1
XDP_BPM#2
XDP_BPM#3
XDP_BPM#4
XDP_BPM#5
XDP_TCK
XDP_TDI
XDP_TDO
XDP_TMS
XDP_TRST#
H_BR#
H_PROCHOT#_CPU
H_PROCHOT_S#
CPU_THRM_DA
CPU_THRM_DC
THRMTRIP#_CPU
PM_THRMTRIP# 11,20,30
CLK_CPU_BCLK
CLK_CPU_BCLK#
H_A20M#
H_FERR#
H_IGNNE#
H_STPCLK#
H_INTR
H_NMI
H_SMI#
H_GTLREF
H_ACLKPH
H_DCLKPH
H_BINIT#
H_EDM
EXTGBREF
H_FORCEPR#
H_HFPLL
H_MCERR#
H_RSP#
CPU_BSEL0
CPU_BSEL1
CPU_BSEL2
H_COMP0
H_COMP1
H_COMP2
H_COMP3
H_DPRSTP# 20,80
H_DPSLP# 20
H_DPWR# 10
H_PWRGD 20
H_CPUSLP# 10,20
CPU_CMREF
H_DPSLP#
H_DPRSTP#
H_PWRGD
H_DPWR#
THRO_CPU
PWRLIMIT_CPU 90
Q0301 2N7002
Q0302 2N7002
E/R V1.1 2008/05/26 R0315 unmount
E/R V1.1 2008/05/26 R0313 unmount
Title : CPU(1)
ASUSTeK COMPUTER INC
Engineer: ENGINEER
Size Custom
Project Name N10
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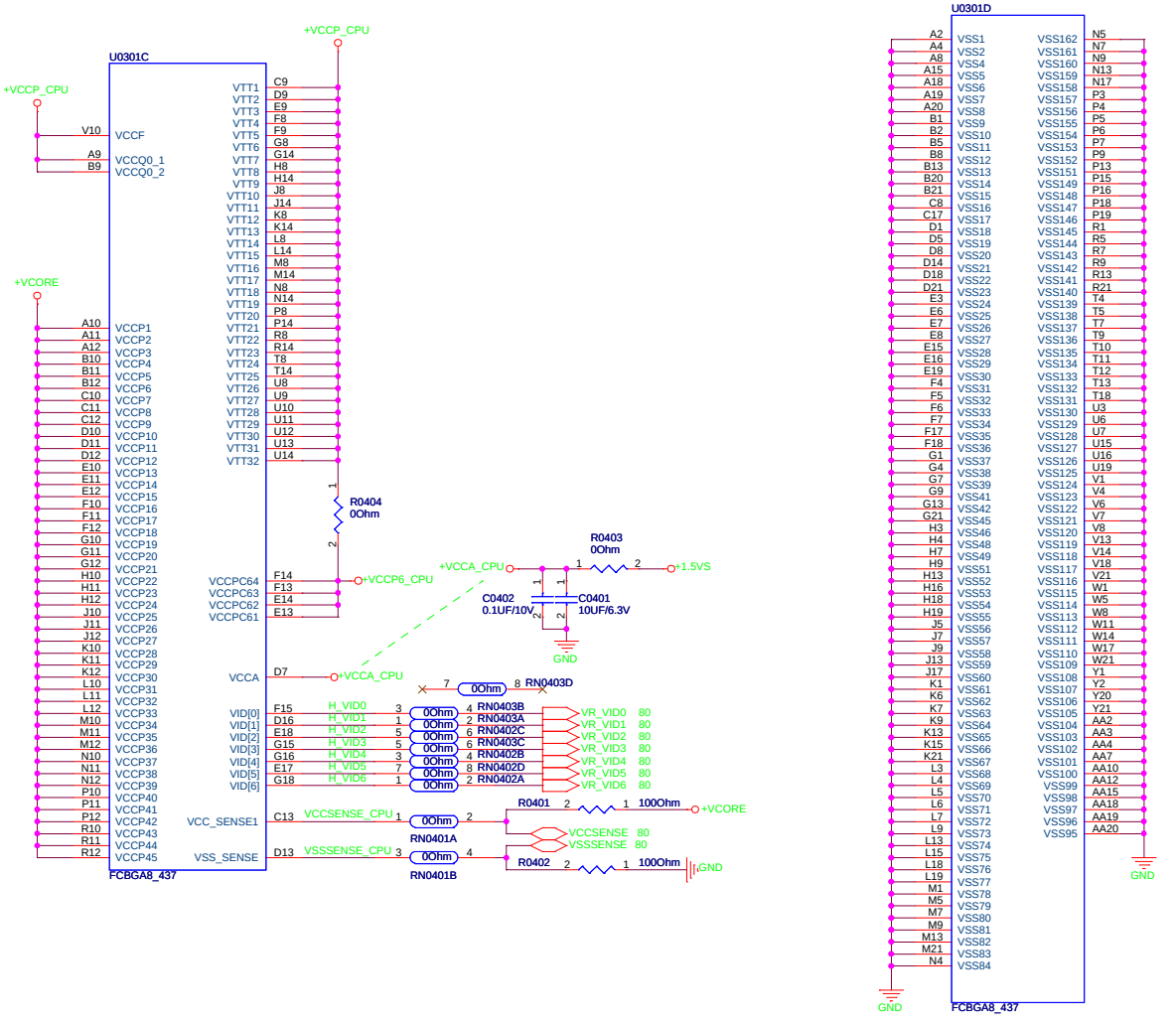

Size	Project Name	Rev
Custom	N10	1.0

Title : CPU(2)

ASUSTeK COMPUTER INC

Engineer: ENGINEER

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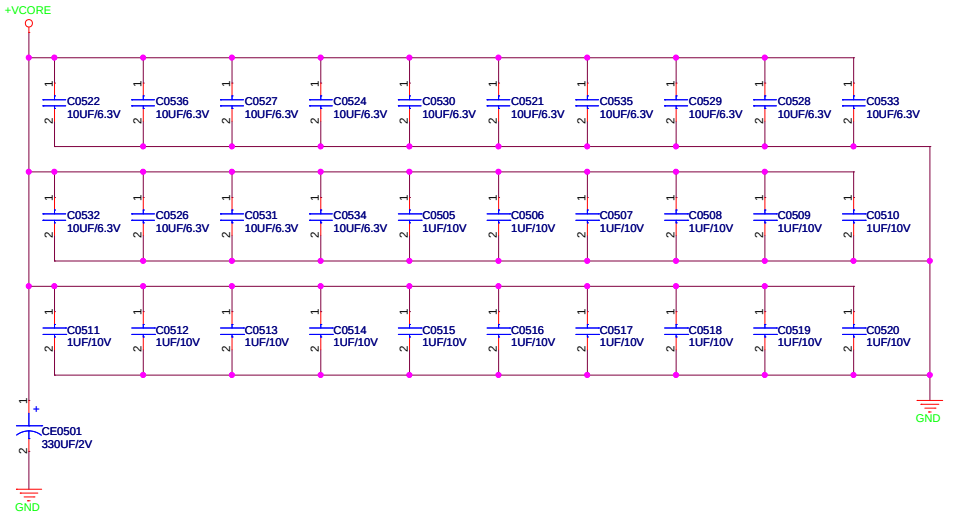
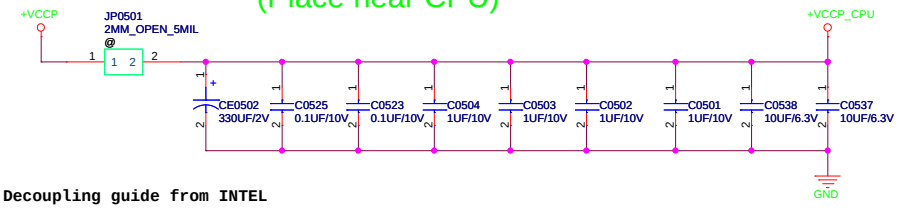
+VCCP Decoupling Capacitor
(Place near CPU)





Decoupling guide from INTEL

VCORE	1uF/10V	* 16pcs for CPU
	10uF/6.3V	*14pcs for CPU
	330uF/2V	* 1pcs for CPU
VCCP	0.1uF	* 2pcs for CPU
	1uF	* 4 pcs for CPU
	10uF	* 2 pcs for CPU
	330uF	* 1pcs for CPU

ASUSTeK COMPUTER INC	Title : CPU CAPS	
	Engineer: ENGINEER	
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ASUSTeK COMPUTER INC	Title : EMPTY	
	Engineer: ENGINEER	
Size: Custom	Project Name: N10	Rev: 1.0
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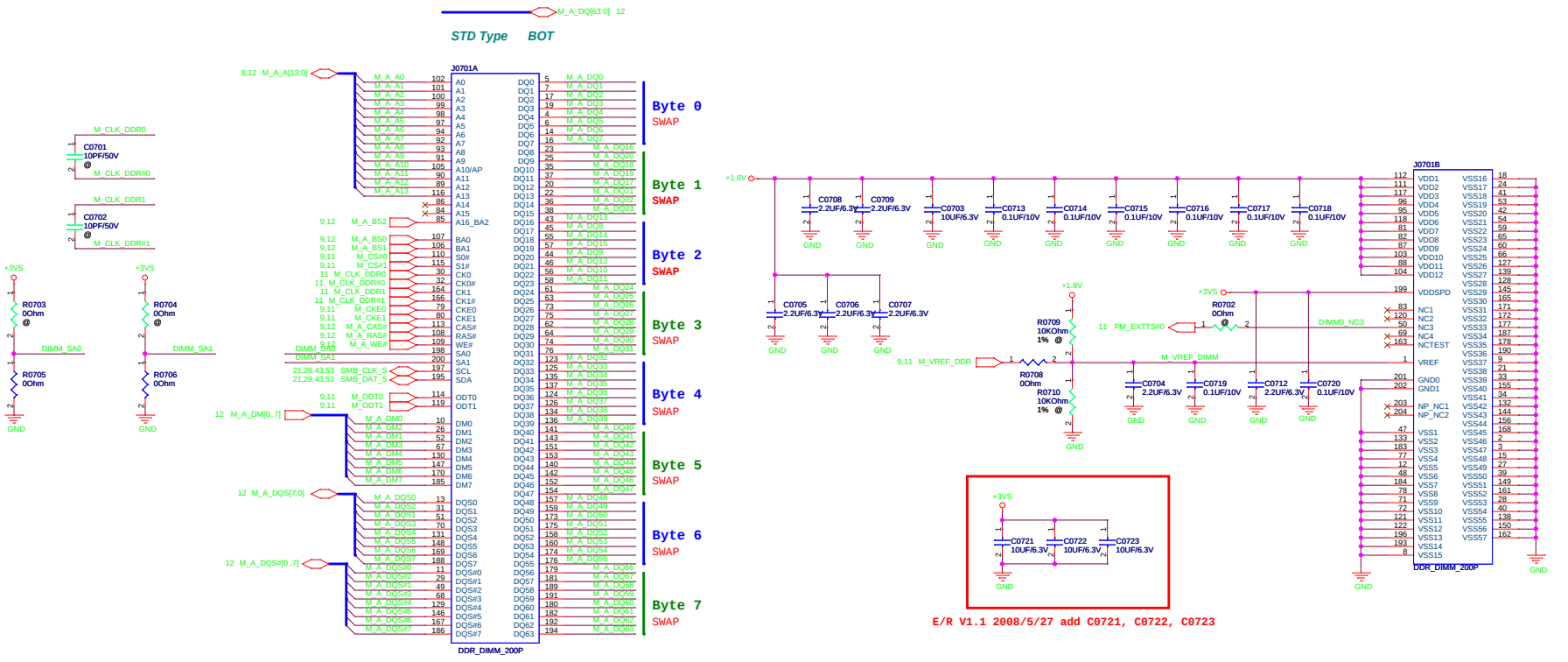

E/R V1.1 2008/5/27 add C0721, C0722, C0723

ASUS	Title : DIMM		
ASUSTeK COMPUTER INC	Engineer: ENGINEER		
Size: Custom	Project Name: N10		Rev: 1.0
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ASUSTeK COMPUTER INC	Title : EMPTY	
	Engineer: ENGINEER	
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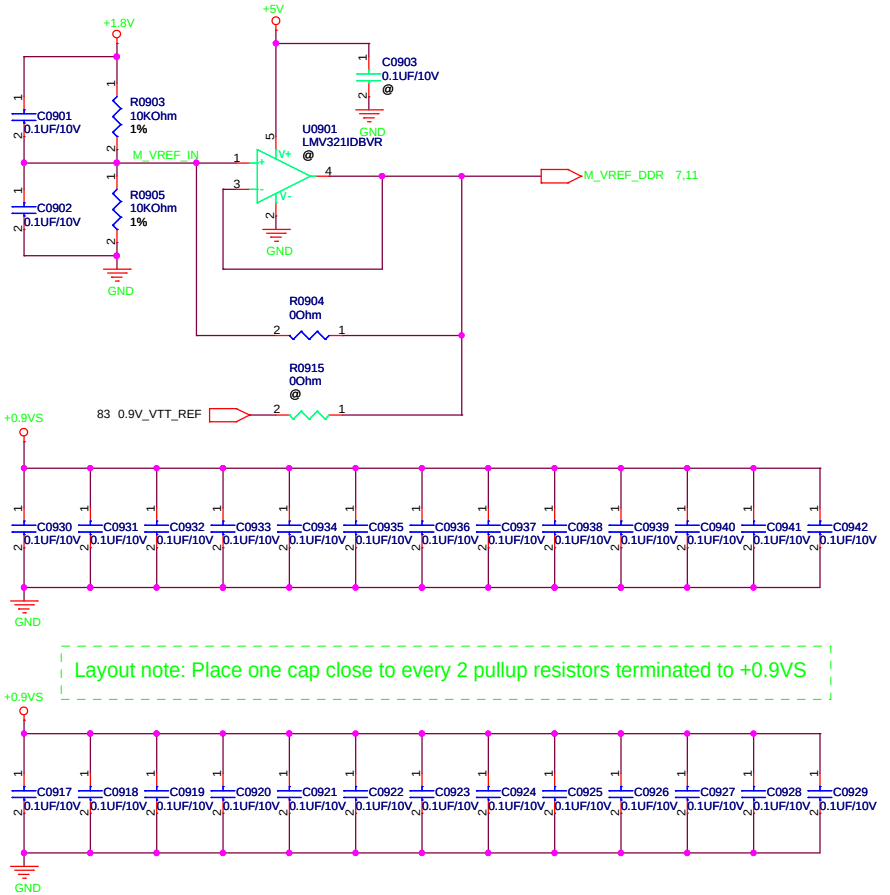
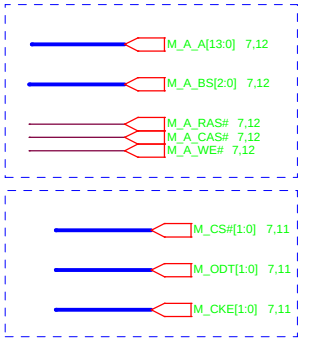
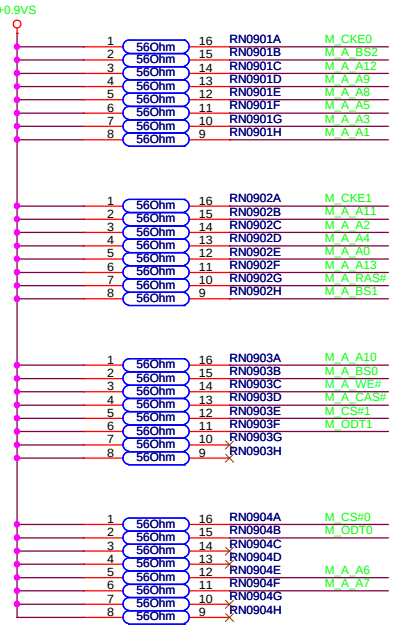


Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS

+0.9VS can be controlled to 0.9V or 0.9VS.
Remind PWR EE to reserve SUSB# and SUSC#



HAD SWAPED



ASUSTeK COMPUTER INC	Title : DDR2 TERM	
	Engineer: ENGINEER	
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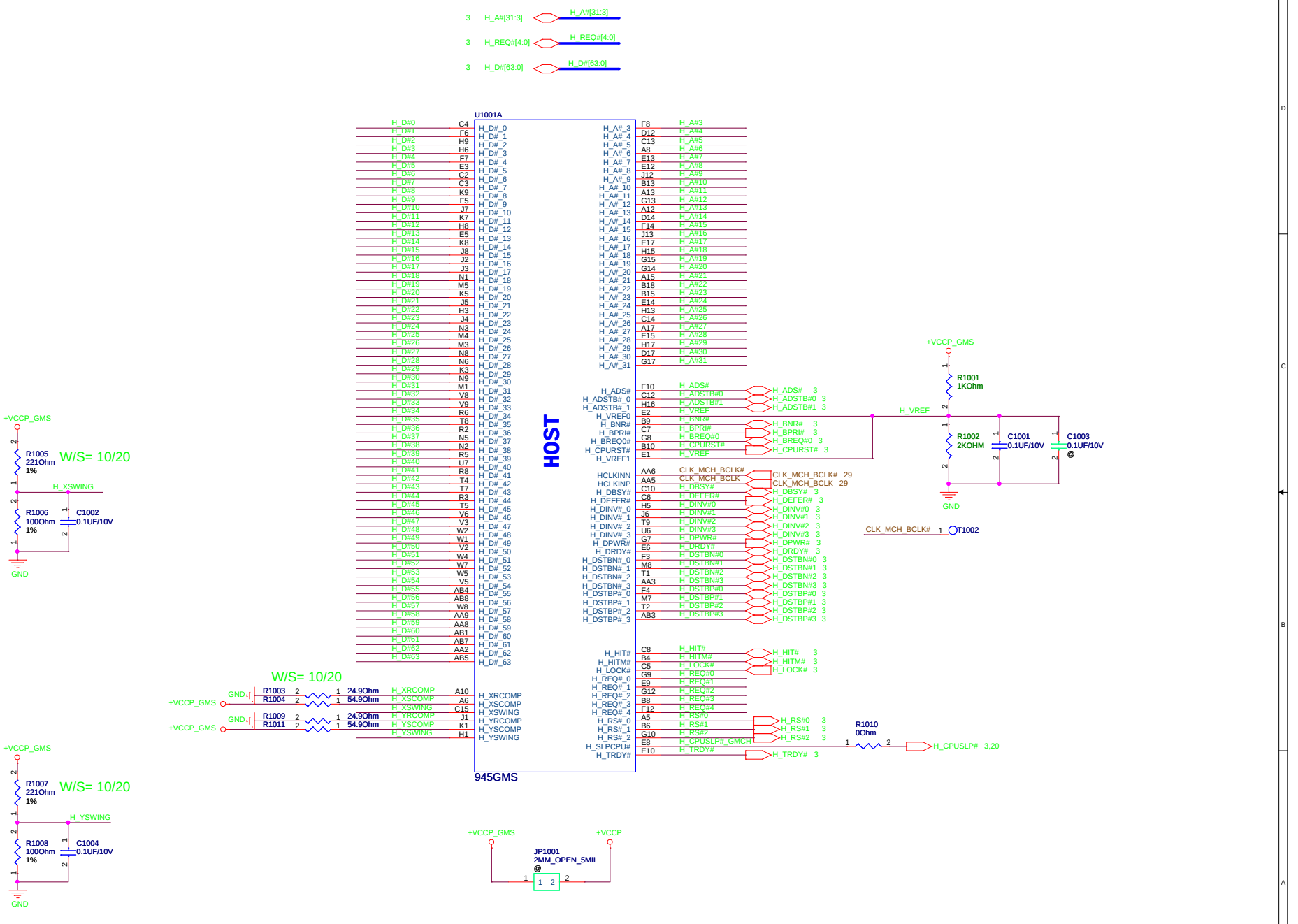

ASUSTeK COMPUTER INC	Title : Calistoga GMCH(1)		
	Engineer: ENGINEER		
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TX/RX of DMI is viewed from ICH7M

Lane Reversal of DMI is not supported in 945GMS

CFG[2:0] :
001=FSB533
011=FSB667

CFG5 : DMI STRAP
LOW = DMI X 2
HIGH =RSVD

CFG[3,6] :
Reserved

U1001B

DMI: DMI_RXN_0 Y29, DMI_RXN_1 Y32, DMI_RXP_0 Y28, DMI_RXP_1 Y31, DMI_TXN_0 V28, DMI_TXN_1 V31, DMI_TXP_0 V29, DMI_TXP_1 V32

DMI2 MUXING: SM_CK_0 AF33, SM_CK_1 AG1, SM_CK_2 AJ1, SM_CK_3 AM30, SM_CK#_0 AG33, SM_CK#_1 AF1, SM_CK#_2 AK1, SM_CK#_3 AN30, SM_CKE_0 AN21, SM_CKE_1 AN22, SM_CKE_2 AF26, SM_CKE_3 AF25, SM_CS#_0 AG14, SM_CS#_1 AF12, SM_CS#_2 AK14, SM_CS#_3 AH12, SM_OCDCOMP_0 AJ21, SM_OCDCOMP_1 AF11, SM_ODT_0 AE12, SM_ODT_1 AF14, SM_ODT_2 AJ14, SM_ODT_3 AJ12, SM_RCOMPN AN12, SM_RCOMPP AN14, SM_VREF_0 AA33, SM_VREF_1 AE1

CFG/RSVD: CFG_0 C18, CFG_1 E18, CFG_2 G20, CFG_3 G18, CFG_5 J20, CFG_6 J18; RESERVED1 K32, RESERVED2 K31, RESERVED7 C17, RESERVED8 F18, RESERVED9 A33

PM: ICH_SYNC# E31, PM_BMBUSY# G21, PM_EXTTS#_0 F26, PM_EXTTS#_1 J15, THRMTRIP# AB29, PWROK W27, RSTIN#

CLK: D_REFCLKINN A27, D_REFCLKINP A26, D_REFSSCLKINN J33, D_REFSSCLKINP H33, CLKREQ# J22

945GMS

21 DMI_TXN0, 21 DMI_TXN1, 21 DMI_TXP0, 21 DMI_TXP1, 21 DMI_RXN0, 21 DMI_RXN1, 21 DMI_RXP0, 21 DMI_RXP1

7 M_CLK_DDR0, 7 M_CLK_DDR1, 7 M_CLK_DDR#0, 7 M_CLK_DDR#1, 7,9 M_CKE0, 7,9 M_CKE1, 7,9 M_CS#0, 7,9 M_CS#1, 7,9 M_ODT0, 7,9 M_ODT1

R1114 40.2Ohm M_OCDCOMP0, R1126 40.2Ohm M_OCDCOMP1

R1111 80.6Ohm M_RCOMPP, R1112 80.6Ohm M_RCOMPN

M_VREF_MCH

MCH_BSEL0 29, MCH_BSEL1 29, MCH_BSEL2 29

R1131 2.2KOhm MCH_CFG3, R1129 2.2KOhm MCH_CFG5, R1130 2.2KOhm MCH_CFG6

R1133 0Ohm MCH_RSVD9

MCH_SYNC# 21, PM_BMBUSY# 21, PM_EXTTS#0, PM_EXTTS#1, THRMTRIP#_GMCH, PM_PWROK_MCH, PLT_RST#_MCH

R1118 0Ohm, R1125 0Ohm, R1127 0Ohm, R1102 100Ohm

PM_DPRSLPVR 21,30, PM_THRMTRIP# 3,30, PM_PWROK 21,30, PLT_RST# 21,33,42

TNTFI 使用 FAST C4E EXIT 不用 FAST C4E EXIT PM_DPRSLPVR 內有內 不准內 R1120 不可以上 R1120 就必須上

CLK_DREFCLK# 29, CLK_DREFCLK 29, CLK_DREFSS# 29, CLK_DREFSS 29, CLK_MCH_REQ# 29

R1116 10KOhm 1% @, R1113 0Ohm, M_VREF_DDR 7,9

C1102 0.1UF/10V @, C1101 0.1UF/10V @, C1103 2.2UF/6.3V @, R1121 10KOhm 1% @

R1119 10KOhm PM_EXTTS#0 — PM_EXTTS#0 7

R1120 10KOhm PM_EXTTS#1 — TNTFI 使用 FAST C4E EXIT 不用 FAST C4E EXIT PM_DPRSLPVR 內有內 不准內 R1120 不可以上 R1120 就必須上

U1001F

MISC: SDVO_CTRLDATA, SDVO_CTRLCLK, G_CLKINN, G_CLKINP

VGA: CRT_DDC_CLK, CRT_DDC_DATA, CRT_BLUE, CRT_BLUE#, CRT_GREEN, CRT_GREEN#, CRT_RED, CRT_RED#, CRT_VSYNC, CRT_HSYNC, CRT_IREF

LVDS: L_BKLTCTL, L_BKLTEN, L_CLKCTLA, L_CTLBDATA, L_DDC_CLK, L_DDC_DATA, L_VDDEN, L_IBG, L_VBG, L_VREFH, L_VREFL, LA_CLKN, LA_CLKP, LB_CLKN, LB_CLKP, LA_DATAN_0, LA_DATAN_1, LA_DATAN_2, LA_DATAP_0, LA_DATAP_1, LA_DATAP_2, LB_DATAN_0, LB_DATAN_1, LB_DATAN_2, LB_DATAP_0, LB_DATAP_1, LB_DATAP_2

SDVO: EXP_A_COMPI R28, EXP_A_ICOMPO M28, SDVO_TVCLKIN# N30, SDVOB_INT# R30, SDVO_FLDSTALL# T29, SDVO_TVCLKIN M30, SDVO_INT P30, SDVO_FLDSTALL T30, SDVO_RED# P28, SDVO_GREEN# N32, SDVO_BLUE# P32, SDVO_CLKN T32, SDVO_RED N28, SDVO_GREEN M32, SDVO_BLUE P33, SDVO_CLKP R32

TV: TV_DACA_OUT A21, TV_DACB_OUT C20, TV_DACC_OUT E20, TV_IREF G23, TV_IRTNA B21, TV_IRTNB C21, TV_IRTNC D21, TV_DCONSEL0 G26, TV_DCONSEL1 J26

945GMS

R1109 10KOhm, T1102

29 CLK_MCH_3GPLL#, 29 CLK_MCH_3GPLL

R1137 10KOhm CRT_DDCCLK_MCH, R1138 10KOhm CRT_DDCDAT_MCH

47 CRT_DDCCLK_MCH, 47 CRT_DDCDAT_MCH, 47 CRT_BLUE_MCH, 47 CRT_GREEN_MCH, 47 CRT_RED_MCH, 47 CRTVSYNC_MCH, 47 CRTHSYNC_MCH

R1139 150Ohm CRT_BLUE_MCH, R1140 150Ohm CRT_GREEN_MCH, R1141 150Ohm CRT_RED_MCH

R1128 255Ohm CRT_IREF

47 LCD_BLADJ_MCH, 47 LCD_BLEN_MCH, 47 EDIDCLK_MCH, 47 EDIDDAT_MCH, 47 LCD_VDDEN_MCH

R1123 10KOhm, R1124 10KOhm, R1135 10KOhm EDIDCLK_MCH, R1136 10KOhm EDIDDAT_MCH

R1122 1.5KOhm, T1103

47 LVDS_LCLKN_MCH, 47 LVDS_LCLKP_MCH, 47 LVDS_L0N_MCH, 47 LVDS_L1N_MCH, 47 LVDS_L2N_MCH, 47 LVDS_L0P_MCH, 47 LVDS_L1P_MCH, 47 LVDS_L2P_MCH

R1101 24.9Ohm 1% PEG_COMP

SDVO DISABLE: SIGNAL BE LEFT NC

TV-OUT DISABLE: SIGNAL/POWER TO 1.5V

ASUSTeK COMPUTER INC	Title : Calistoga GMCH (2)		
	Engineer: ENGINEER		
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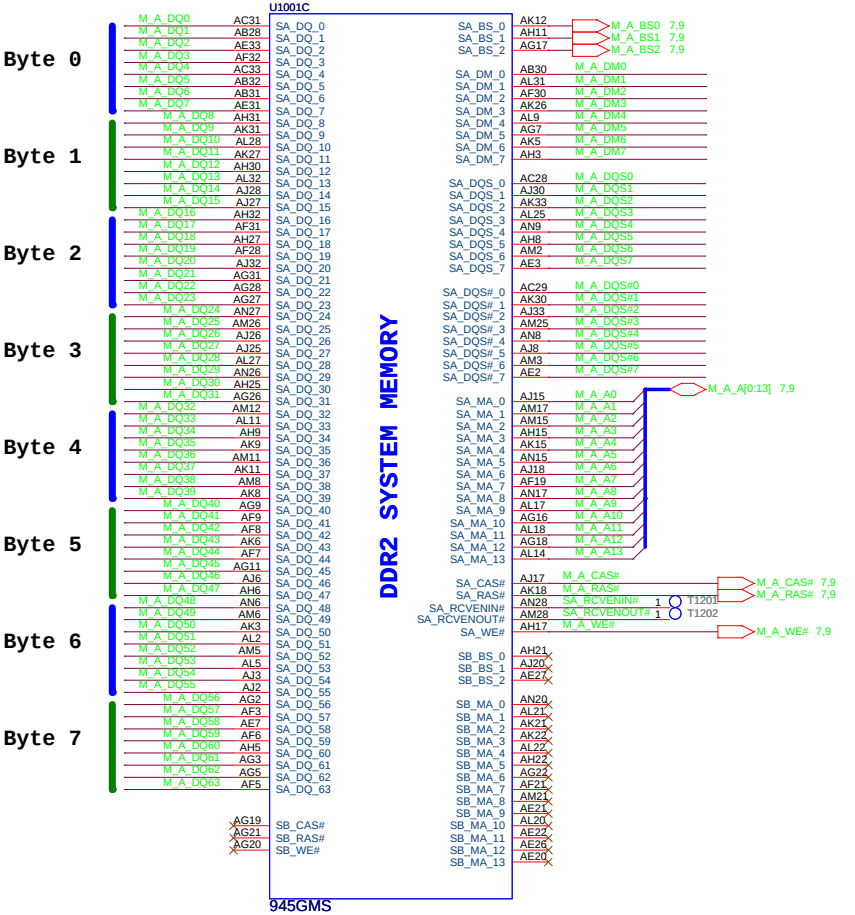

ASUSTeK COMPUTER INC	Title : Calistoga GMCH (3)	Engineer: ENGINEER
Size: Custom	Project Name: N10	Rev: 1.0
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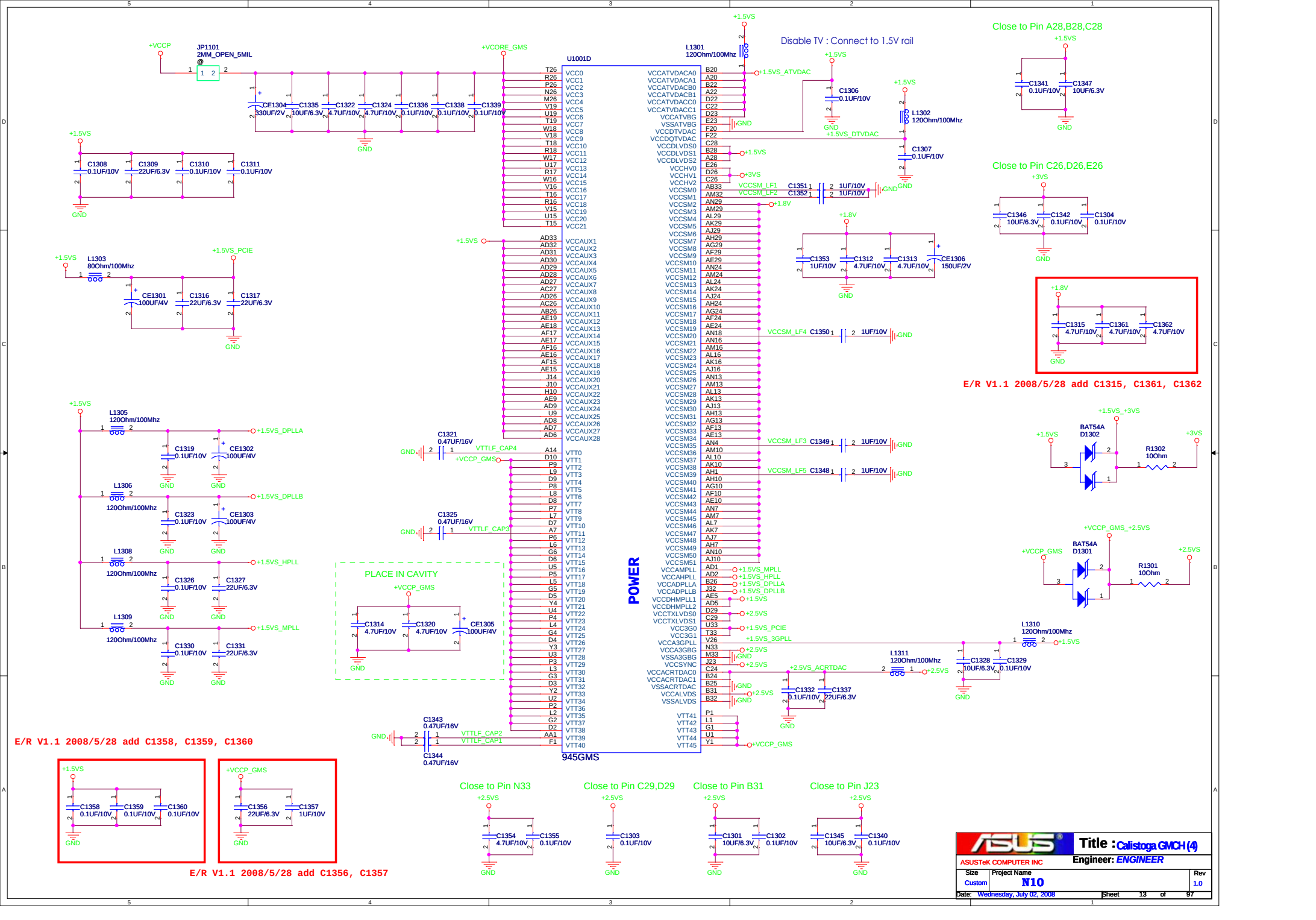
U1001D
945GMS
POWER
JP1101
2MM_OPEN_5MIL
+VCCP
+VCORE_GMS
L1301
120Ohm/100Mhz
Disable TV : Connect to 1.5V rail
Close to Pin A28,B28,C28
Close to Pin C26,D26,E26
L1302
120Ohm/100Mhz
L1303
80Ohm/100Mhz
+1.5VS_PCIE
+1.5VS_ATVDAC
+1.5VS_DTVDAC
VCCSM_LF1
VCCSM_LF2
VCCSM_LF4
VCCSM_LF3
VCCSM_LF5
E/R V1.1 2008/5/28 add C1315, C1361, C1362
L1305
120Ohm/100Mhz
+1.5VS_DPLLA
L1306
120Ohm/100Mhz
+1.5VS_DPLLB
L1308
120Ohm/100Mhz
+1.5VS_HPLL
L1309
120Ohm/100Mhz
+1.5VS_MPLL
VTTLF_CAP4
VTTLF_CAP3
VTTLF_CAP2
VTTLF_CAP1
PLACE IN CAVITY
BAT54A
D1302
D1301
R1302
10Ohm
R1301
10Ohm
+1.5VS_+3VS
+VCCP_GMS_+2.5VS
+2.5VS_ACRTDAC
+2.5VS_3GPLL
L1310
120Ohm/100Mhz
L1311
120Ohm/100Mhz
E/R V1.1 2008/5/28 add C1358, C1359, C1360
E/R V1.1 2008/5/28 add C1356, C1357
Close to Pin N33
Close to Pin C29,D29
Close to Pin B31
Close to Pin J23
Title : Calistoga GMCH (4)
ASUSTeK COMPUTER INC
Engineer: ENGINEER
Size
Custom
Project Name
N10
Rev
1.0
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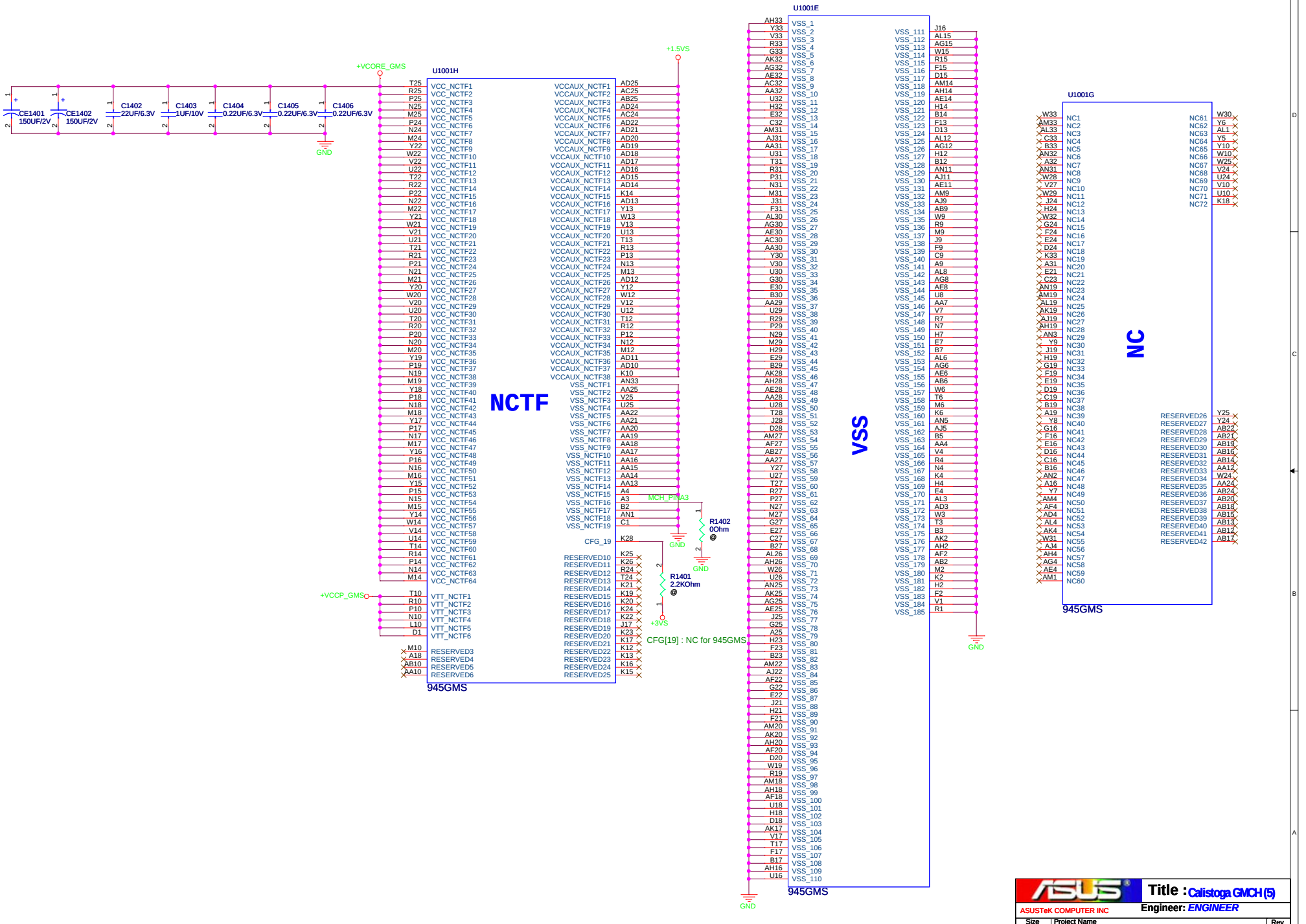

Title : Calistoga GMCH (5)		
ASUSTeK COMPUTER INC	Engineer: ENGINEER	
Size: Custom	Project Name: N10	Rev: 1.0
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ASUSTeK COMPUTER INC	Title : EMPTY		
	Engineer: ENGINEER		
Size: A	Project Name: N10		Rev: 1.0
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ASUSTeK COMPUTER INC	Title : EMPTY	
	Engineer: ENGINEER	
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ASUSTeK COMPUTER INC	Title : EMPTY	
	Engineer: ENGINEER	
Size: A	Project Name: N10	Rev: 1.0
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ASUSTeK COMPUTER INC	Title : EMPTY		
	Engineer: ENGINEER		
Size: A	Project Name: N10		Rev: 1.0
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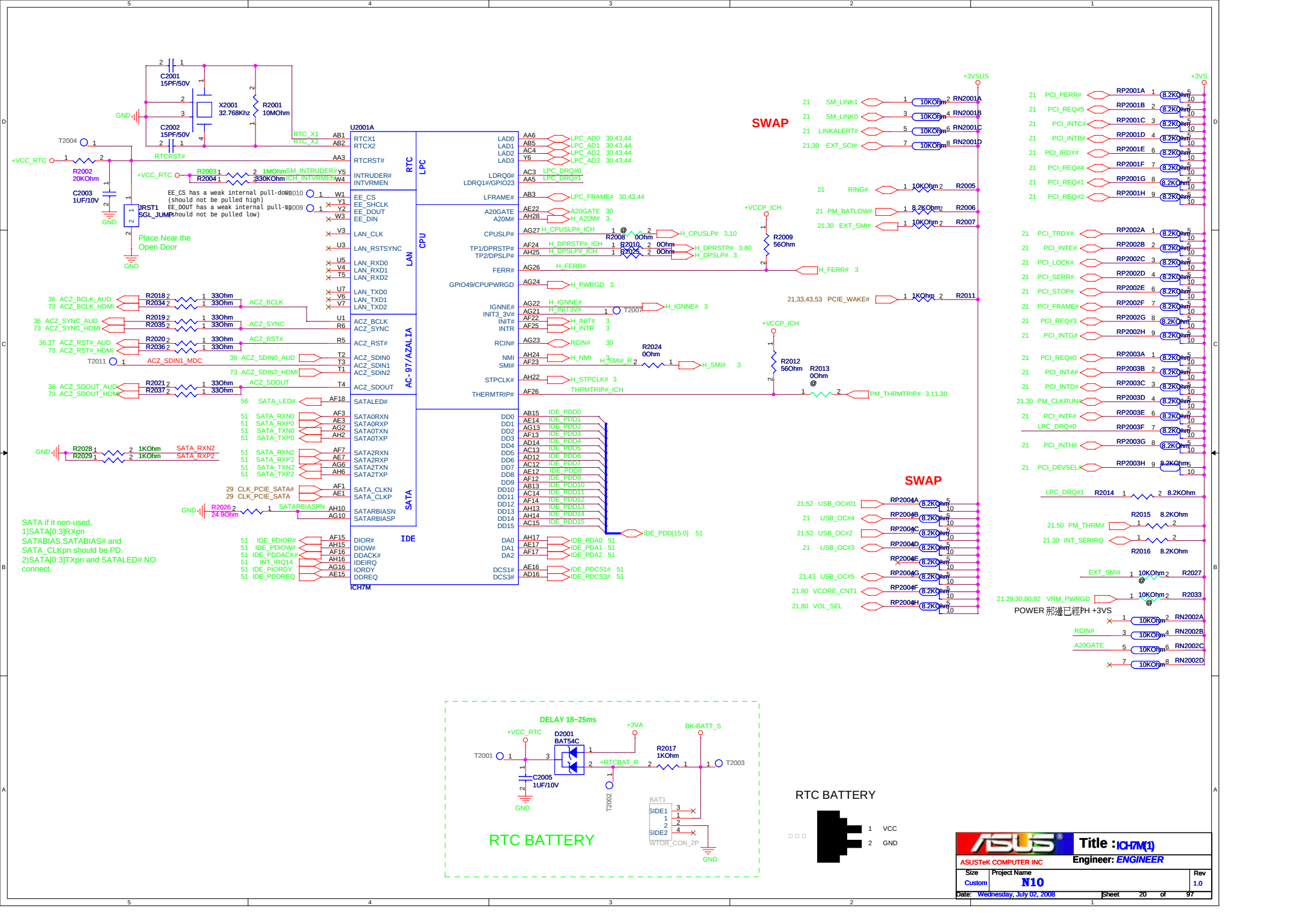
Title : EMPTY			
ASUSTeK COMPUTER INC	Engineer: ENGINEER		
Size: A	Project Name: N10		Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 19 of 97		


U2001A
RTC
LPC
CPU
LAN
AC-97/AZALIA
SATA
IDE
ICH7M
C2001 15PF/50V
C2002 15PF/50V
X2001 32.768Khz
R2001 10MOhm
R2002 20KOhm
C2003 1UF/10V
JRST1 SGL_JUMP
Place Near the Open Door
EE_CS has a weak internal pull-down (should not be pulled high)
EE_DOUT has a weak internal pull-up (should not be pulled low)
SATA if it non-used,
1)SATA[0:3]RXpn SATABIAS,SATABIAS# and SATA_CLKpn should be PD.
2)SATA[0:3]TXpn and SATALED# NO connect.
SWAP
SWAP
POWER 那邊已經PH +3VS
DELAY 18~25ms
D2001 BAT54C
R2017 1KOhm
C2005 1UF/10V
RTC BATTERY
RTC BATTERY
1 VCC
2 GND
Title : ICH7M(1)
ASUSTeK COMPUTER INC
Engineer: ENGINEER
Size Custom
Project Name N10
Rev 1.0
Date: Wednesday, July 02, 2008
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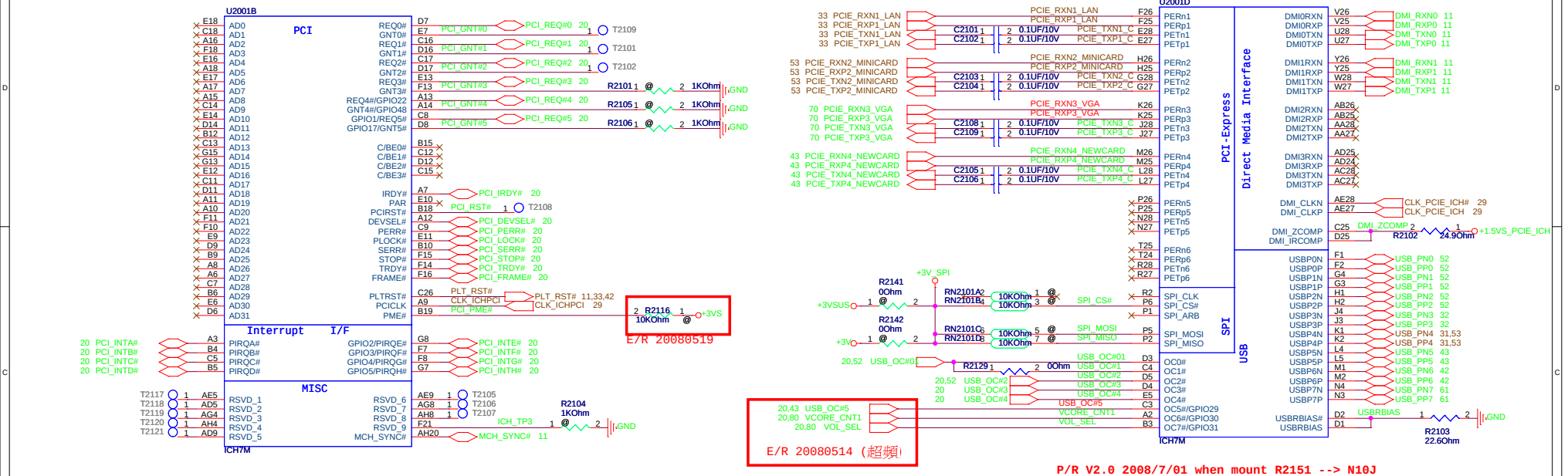
ICH7 Boot BIOS select

	GNT#5	GNT#4	
LPC	1	1	(default)
PCI	1	0	
SPI	0	1	

GNT#3 without PD, it NOT top-block swap(inter high)

PCIE TX/RX 方向命名是以 ICH7M 爲中心

TX/RX of DMI is viewed from ICH7M
Lane Reversal of DMI is not supported in 945GMS



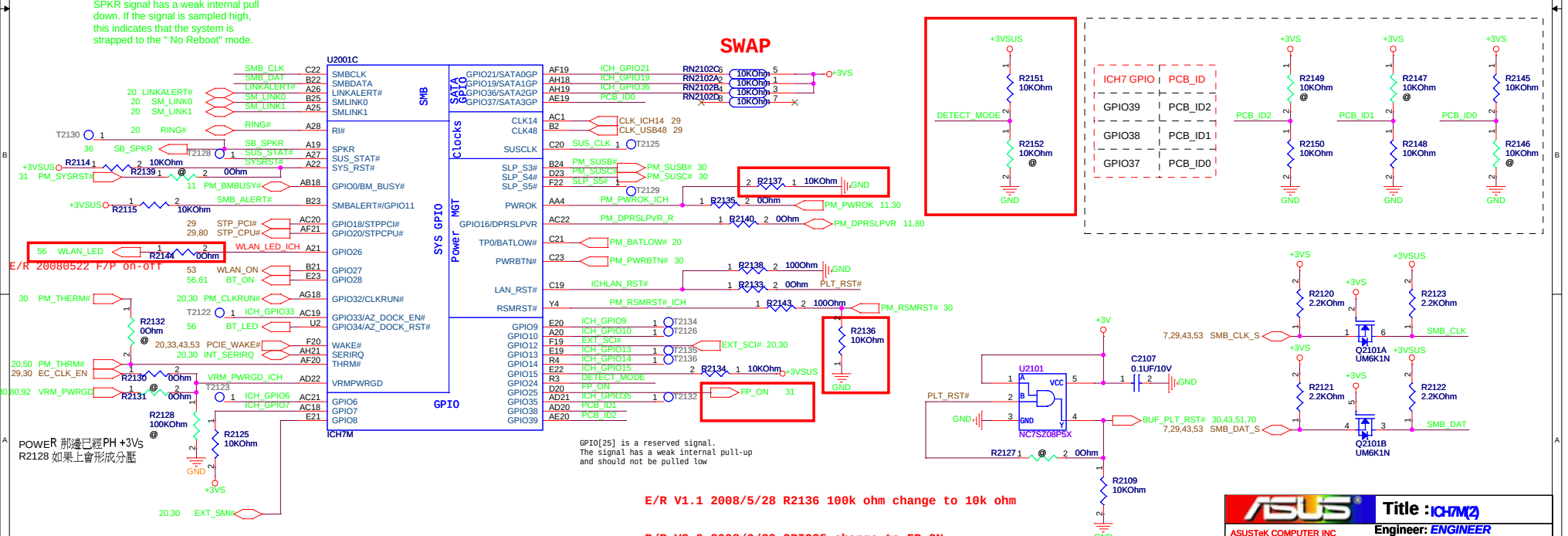
E/R V1.1 2008/5/28 R2137 100k ohm change to 10k ohm

P/R V2.0 2008/7/01 when mount R2151 --> N10J

P/R V2.0 2008/7/01 when mount R2152 --> N10E

SPKR signal has a weak internal pull down. If the signal is sampled high, this indicates that the system is strapped to the " No Reboot" mode.

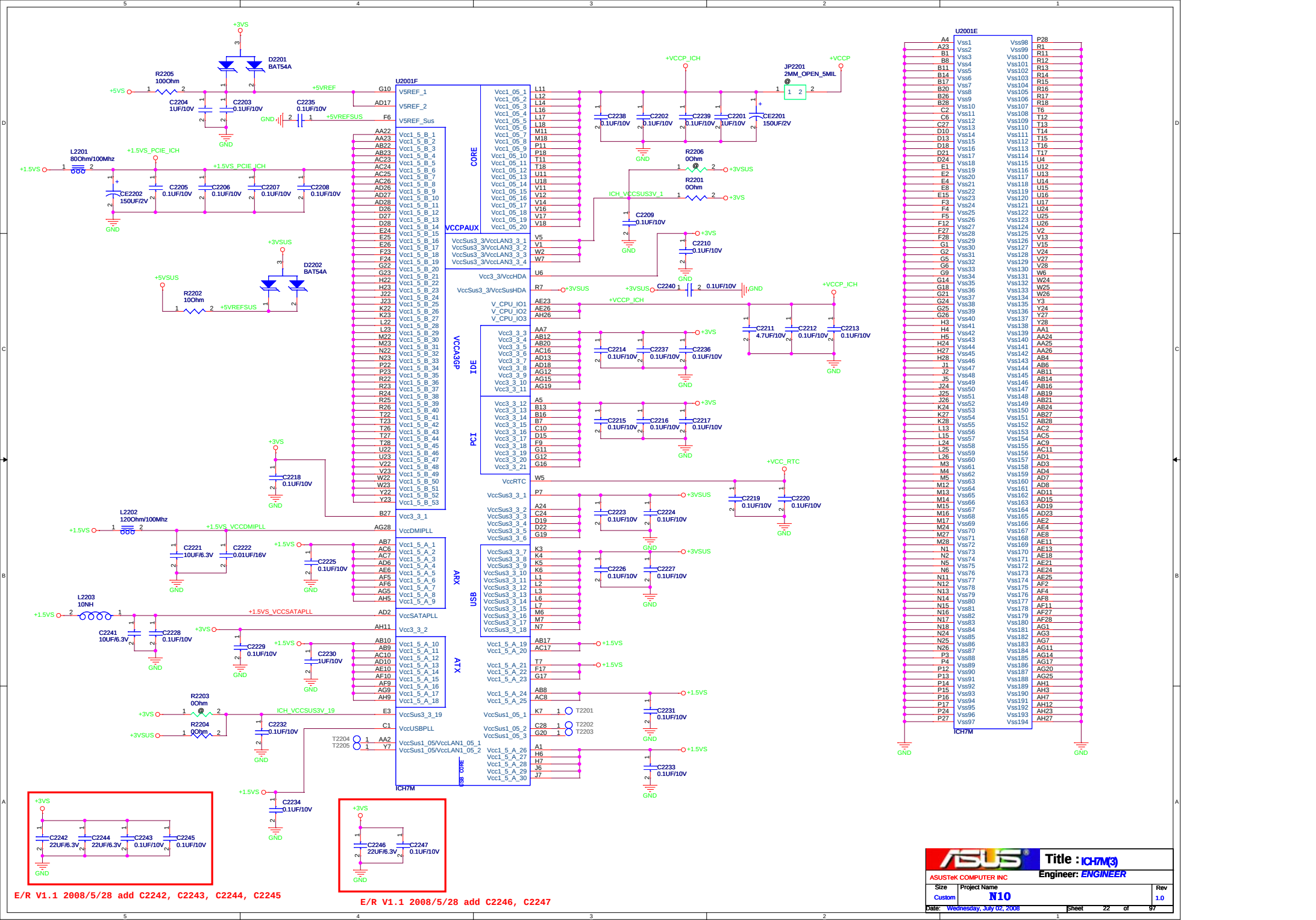
SWAP



E/R V1.1 2008/5/28 R2136 100k ohm change to 10k ohm

P/R V2.0 2008/6/29 GPIO25 change to FP_ON

ASUSTeK COMPUTER INC	Title : ICH7M(2)		
	Engineer: ENGINEER		
Size: Custom	Project Name: N10		Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 21 of 97		



ASUSTeK COMPUTER INC	Title : ICH7M(3)		
	Engineer: ENGINEER		
Size: Custom	Project Name: N10	Rev: 1.0	
Date: Wednesday, July 02, 2008	Sheet 22 of 97		

ASUSTeK COMPUTER INC	Title : EMPTY	
	Engineer: ENGINEER	
Size: A	Project Name: N10	Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 23 of 97	

ASUSTeK COMPUTER INC	Title : EMPTY	
	Engineer: ENGINEER	
Size: A	Project Name: N10	Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 24 of 97	

ASUSTeK COMPUTER INC	Title : EMPTY	
	Engineer: ENGINEER	
Size: A	Project Name: N10	Rev: 1.0
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Title : EMPTY			
ASUSTeK COMPUTER INC	Engineer: ENGINEER		
Size: A	Project Name: N10		Rev: 1.0
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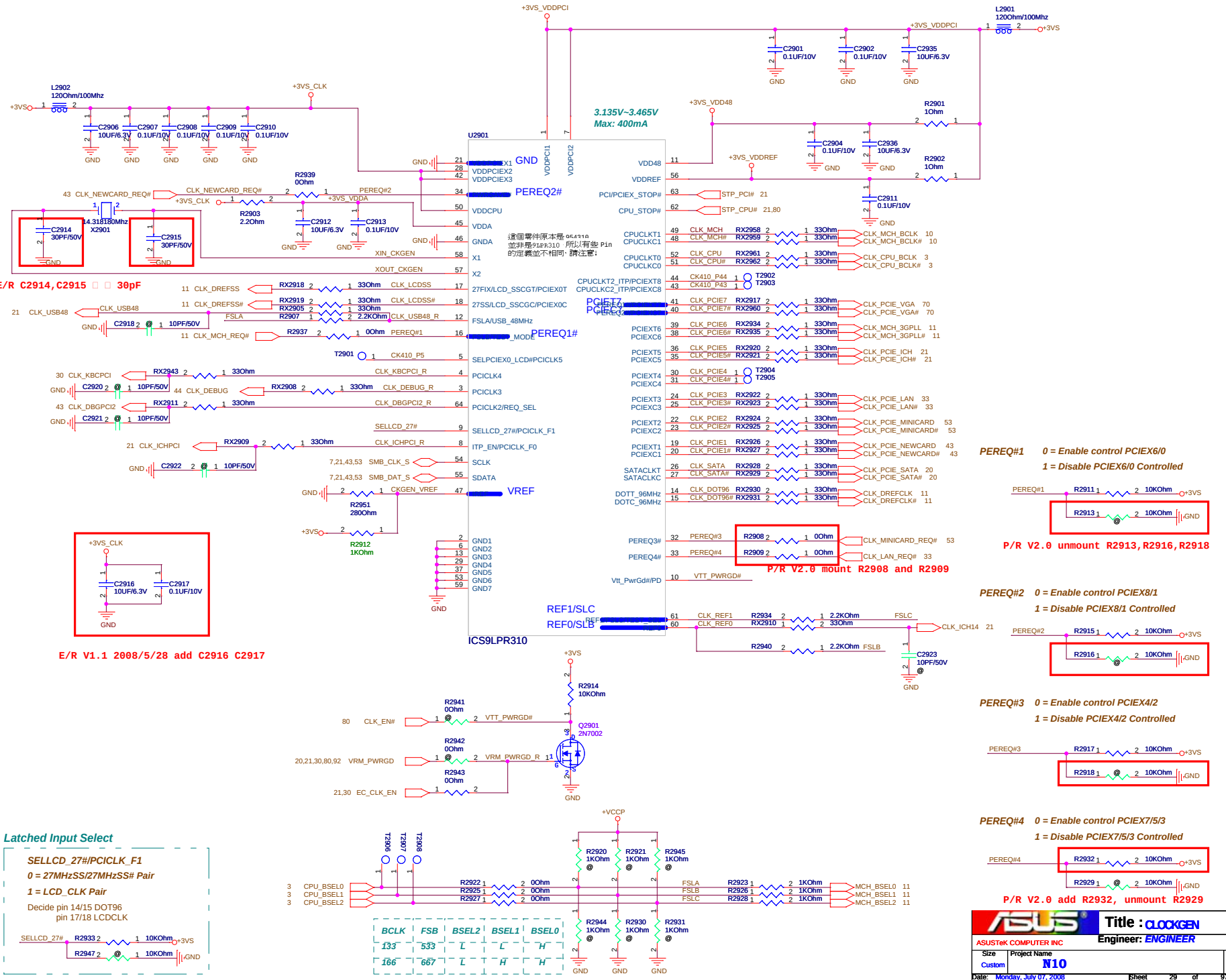
ASUSTeK COMPUTER INC	Title : EMPTY		
	Engineer: ENGINEER		
Size: A	Project Name: N10		Rev: 1.0
Date: Wednesday, July 02, 2008		Sheet 27 of 97	

ASUSTeK COMPUTER INC	Title : EMPTY		
	Engineer: ENGINEER		
Size: A	Project Name: N10		Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 28 of 97		


U2901
ICS9LPR310
3.135V~3.465V
Max: 400mA
這個零件原本是 PCI2310
並非是91LPR310 所以有些 Pin
的定義並不相同，請注意!
E/R C2914,C2915 30pF
E/R V1.1 2008/5/28 add C2916 C2917
P/R V2.0 mount R2908 and R2909
P/R V2.0 unmount R2913,R2916,R2918
P/R V2.0 add R2932, unmount R2929
PEREQ#1 0 = Enable control PCIEX6/0
1 = Disable PCIEX6/0 Controlled
PEREQ#2 0 = Enable control PCIEX8/1
1 = Disable PCIEX8/1 Controlled
PEREQ#3 0 = Enable control PCIEX4/2
1 = Disable PCIEX4/2 Controlled
PEREQ#4 0 = Enable control PCIEX7/5/3
1 = Disable PCIEX7/5/3 Controlled
Latched Input Select
SELLCD_27#/PCICLK_F1
0 = 27MHzSS/27MHzSS# Pair
1 = LCD_CLK Pair
Decide pin 14/15 DOT96
pin 17/18 LCDCLK
BCLK FSB BSEL2 BSEL1 BSEL0
133 533 L L H
166 667 L H H
Title : CLOCKGEN
Engineer: ENGINEER
ASUSTeK COMPUTER INC
Size Custom
Project Name N10
Rev 1.0
Date: Monday, July 07, 2008
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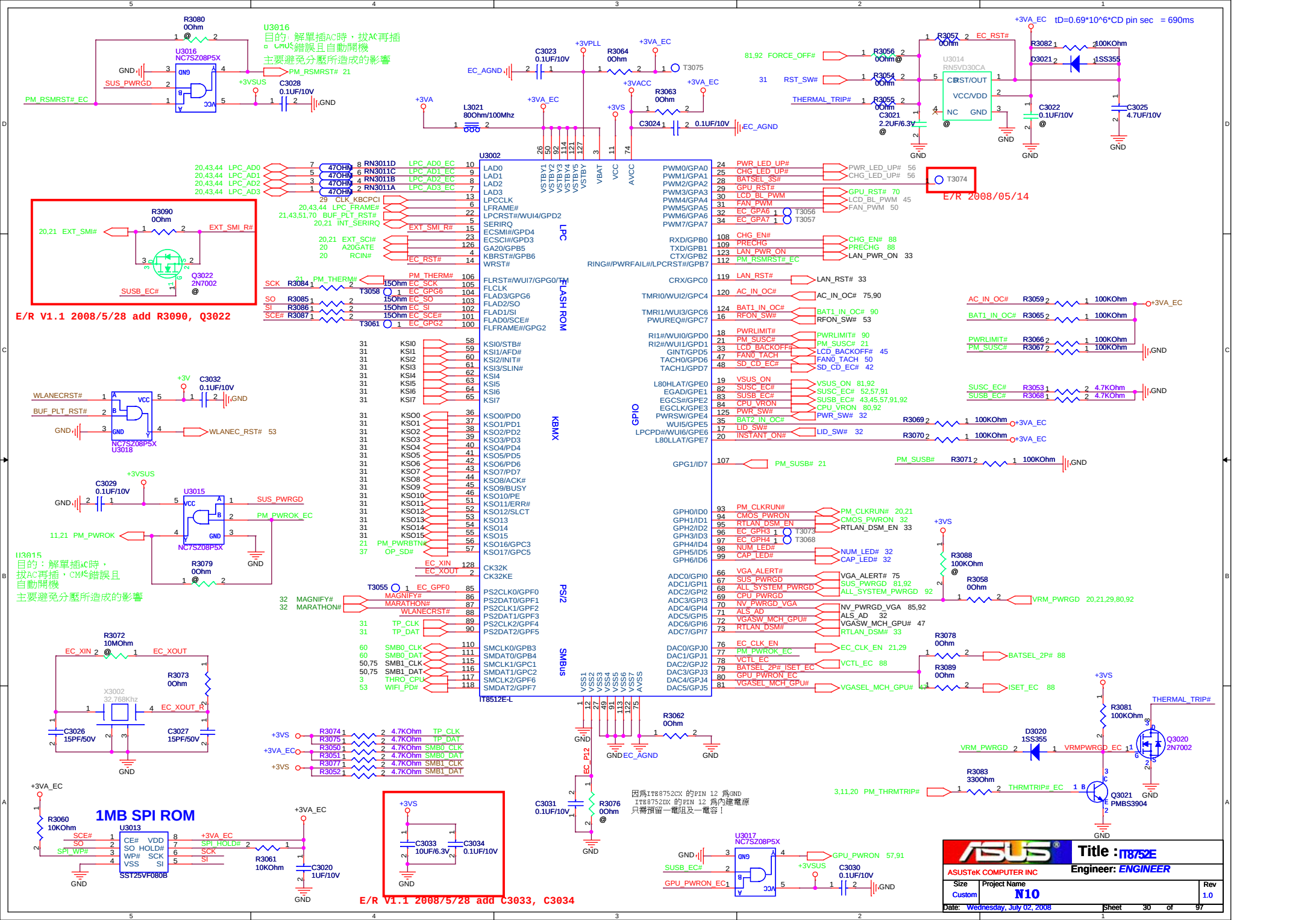
U3016
目的：解單插AC時，拔AC再插
CMOS錯誤且自動開機
主要避免分壓所造成的影響
U3016
目的：解單插AC時，
拔AC再插，CMOS錯誤且
自動開機
主要避免分壓所造成的影響
tD=0.69*10^6*CD pin sec = 690ms
E/R 2008/05/14
E/R V1.1 2008/5/28 add R3090, Q3022
E/R V1.1 2008/5/28 add C3033, C3034
1MB SPI ROM
因爲ITE8752CX 的PIN 12 爲GND
ITE8752DX 的PIN 12 爲內建電源
只需預留一電阻及一電容！
U3002
IT8512E-L
LPC
FLASH ROM
KBMX
PS/2
SMBus
GPIO
Title : IT8752E
ASUSTeK COMPUTER INC
Engineer: ENGINEER
Size Custom
Project Name N10
Rev 1.0
Date: Wednesday, July 02, 2008
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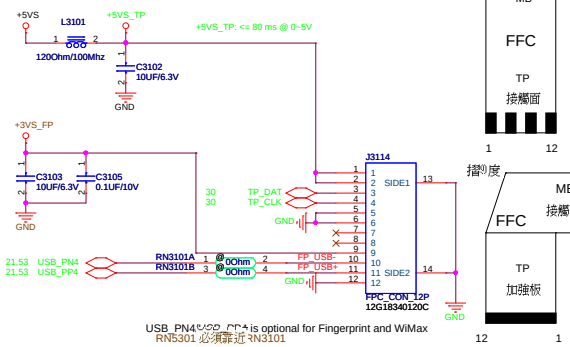
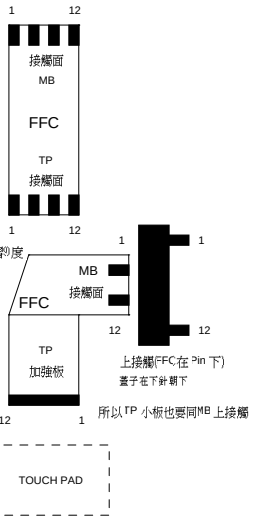
TOUCHPAD FPC

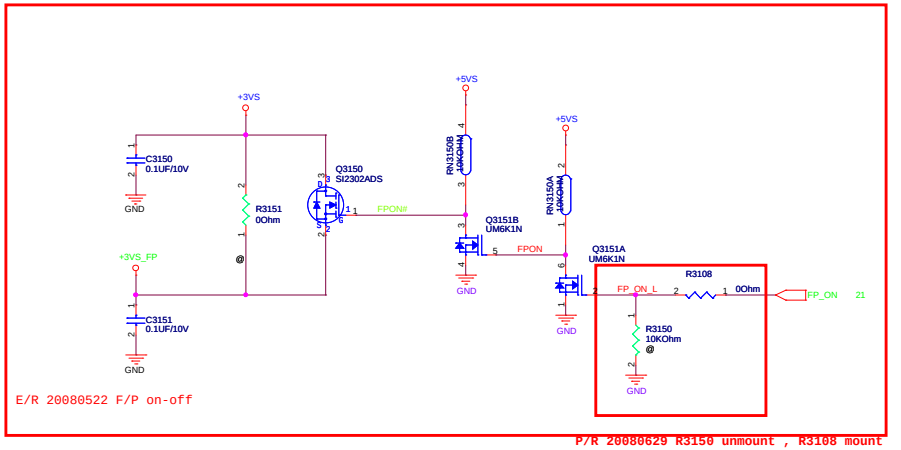


USB_PN4&PP4 is optional for Fingerprint and WiMax
RN5301 必須靠近 RN3101



TOUCH PAD

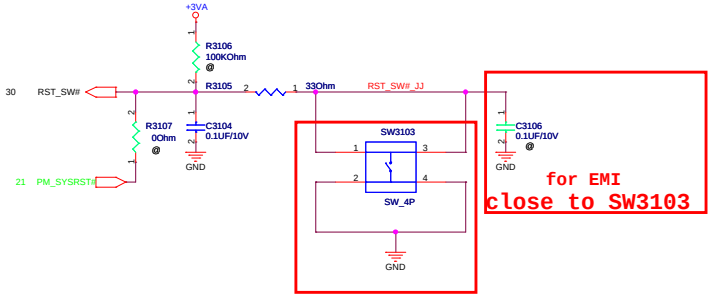
製作FFC 時要提醒ME標示TP/MB 文字面以利組裝

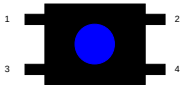


E/R 20080522 F/P on-off

P/R 20080629 R3150 unmount , R3108 mount

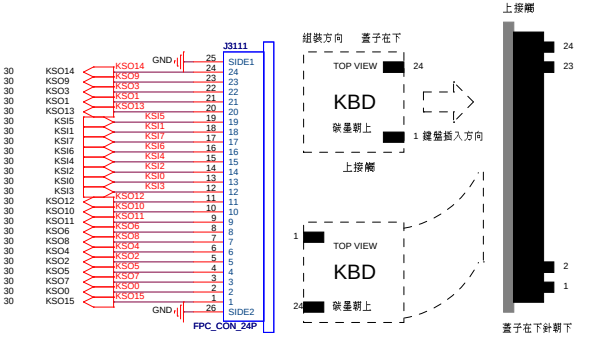
RESET BUTTON

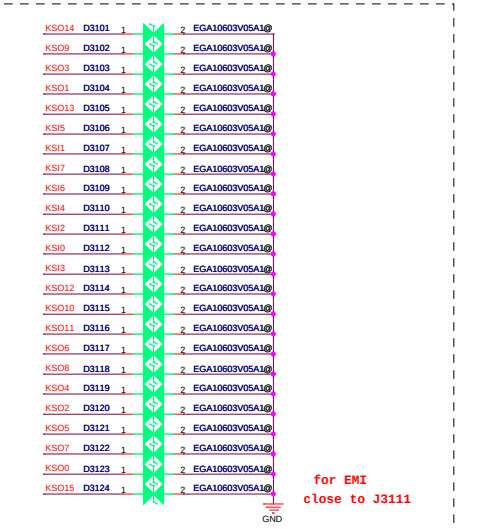




P/R 20080625 SW3103 change P/N

INTERNAL KEYBOARD

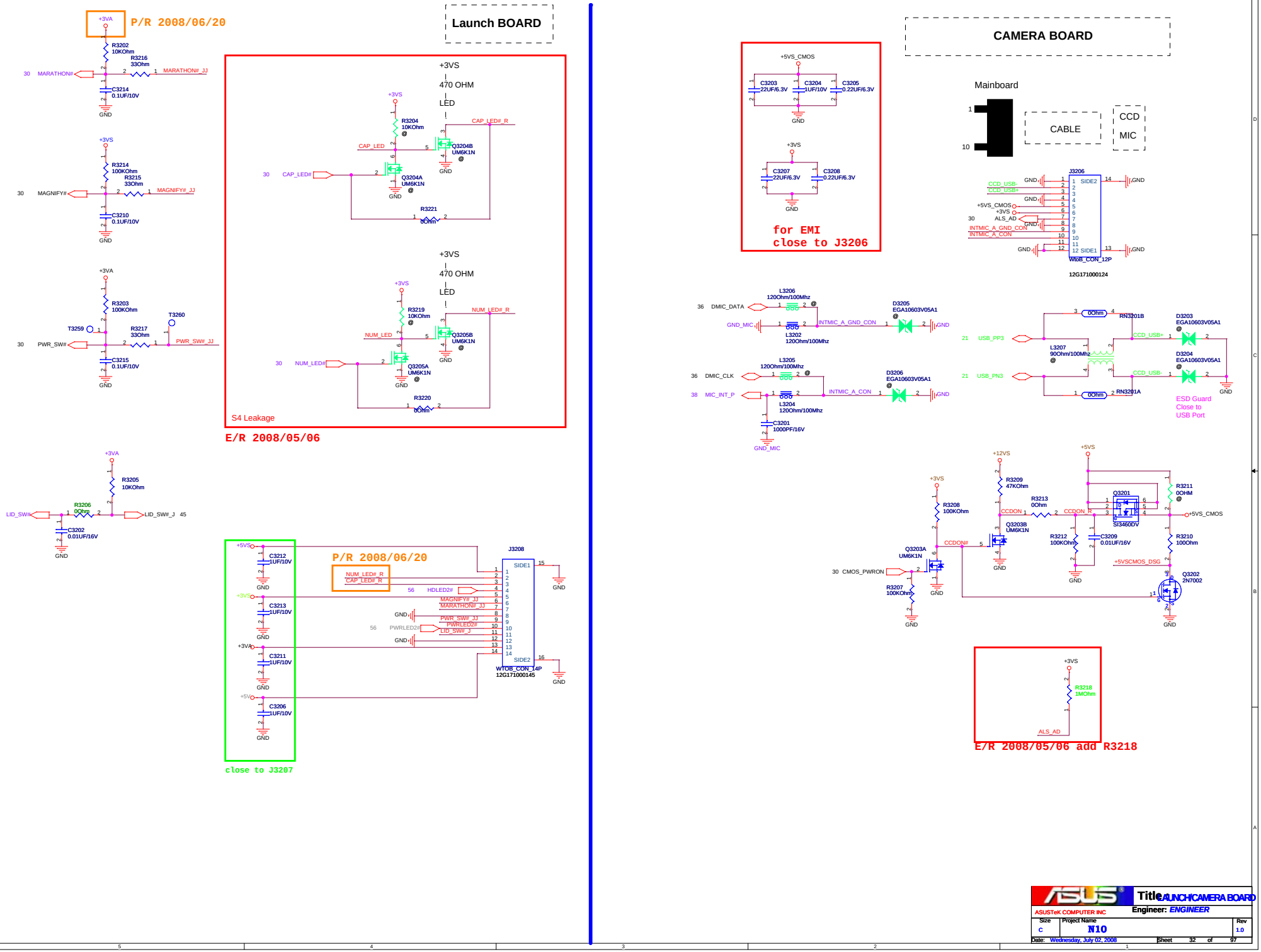




for EMI
close to J3111

爲使Layout 簡潔ESD在BOM可改成同包裝0603電容

ASUSTeK COMPUTER INC	Title : KEYBOARD	
	Engineer: ENGINEER	
Size C	Project Name N10	Rev 1.0
Date: Wednesday, July 02, 2008	Sheet 31 of 97	


Launch BOARD
P/R 2008/06/20
+3VA
R3202 10KOhm
R3216 33Ohm
30 MARATHON#
MARATHON# JJ
C3214 0.1UF/10V
GND
+3VS
R3214 100KOhm
R3215 33Ohm
30 MAGNIFY#
MAGNIFY# JJ
C3210 0.1UF/10V
+3VA
R3203 100KOhm
T3259
T3260
R3217 33Ohm
30 PWR_SW#
PWR_SW# JJ
C3215 0.1UF/10V
+3VA
R3205 10KOhm
R3206 0Ohm
LID_SW#
LID_SW# J 45
C3202 0.01UF/16V
+3VS
470 OHM
LED
R3204 10Ohm @
CAP_LED# R
CAP_LED
Q3204B UM6K1N @
30 CAP_LED#
Q3204A UM6K1N @
R3221 0Ohm
+3VS
470 OHM
LED
R3219 10Ohm @
NUM_LED# R
NUM_LED
Q3205B UM6K1N @
30 NUM_LED#
Q3205A UM6K1N @
R3220 0Ohm
S4 Leakage
E/R 2008/05/06
+5VS
C3212 1UF/10V
+3VS
C3213 1UF/10V
+3VA
C3211 1UF/10V
+5V
C3206 1UF/10V
P/R 2008/06/20
NUM_LED# R
CAP_LED# R
56 HDLED2#
MAGNIFY# JJ
MARATHON# JJ
PWR_SW# JJ
56 PWRLED2#
PWRLED2#
LID_SW# J
J3208
SIDE1
SIDE2
WTOB_CON_14P
12G171000145
close to J3207
CAMERA BOARD
+5VS_CMOS
C3203 22UF/6.3V
C3204 1UF/10V
C3205 0.22UF/6.3V
+3VS
C3207 22UF/6.3V
C3208 0.22UF/6.3V
for EMI
close to J3206
Mainboard
CABLE
CCD
MIC
J3206
CCD_USB-
CCD_USB+
+5VS_CMOS
+3VS
30 ALS_AD
INTMIC_A_GND_CON
INTMIC_A_CON
SIDE2
SIDE1
WTOB_CON_12P
12G171000124
36 DMIC_DATA
L3206 120Ohm/100Mhz
GND_MIC
L3202 120Ohm/100Mhz
INTMIC_A_GND_CON
D3205 EGA10603V05A1 @
36 DMIC_CLK
L3205 120Ohm/100Mhz
38 MIC_INT_P
L3204 120Ohm/100Mhz
C3201 1000PF/16V
INTMIC_A_CON
D3206 EGA10603V05A1 @
21 USB_PP3
21 USB_PN3
L3207 90Ohm/100Mhz @
0Ohm
RN3201B
RN3201A
D3203 EGA10603V05A1 @
D3204 EGA10603V05A1 @
CCD_USB+
CCD_USB-
ESD Guard
Close to
USB Port
+12VS
+5VS
R3209 47KOhm
R3208 100KOhm
R3213 0Ohm
CCDON
CCDON_R
Q3203B UM6K1N
CCDON#
Q3203A UM6K1N
30 CMOS_PWRON
R3207 100KOhm
Q3201 SI3460DV
R3211 0OHM @
+5VS_CMOS
R3212 100KOhm
C3209 0.01UF/16V
R3210 100Ohm
+5VSCMOS_DSG
Q3202 2N7002
+3VS
R3218 1MOhm
ALS_AD
E/R 2008/05/06 add R3218
ASUSTeK COMPUTER INC
Title: LAUNCHCAMERA BOARD
Engineer: ENGINEER
Size C
Project Name N10
Rev 1.0
Date: Wednesday, July 02, 2008
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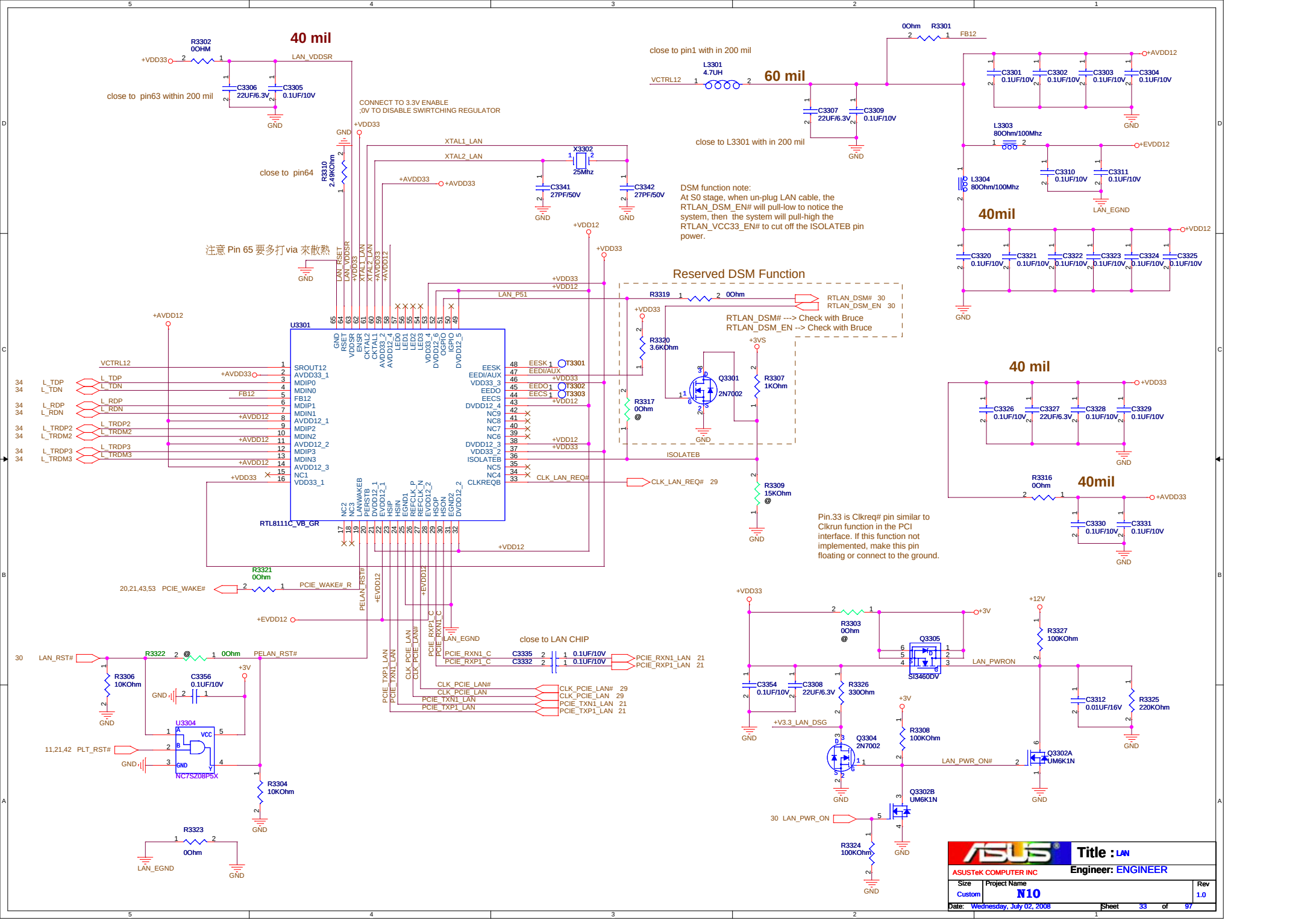
40 mil
R3302 0OHM
+VDD33
LAN_VDDSR
C3306 22UF/6.3V
C3305 0.1UF/10V
close to pin63 within 200 mil
GND
CONNECT TO 3.3V ENABLE
;0V TO DISABLE SWIRTCHING REGULATOR
close to pin1 with in 200 mil
L3301 4.7UH
VCTRL12
60 mil
C3307 22UF/6.3V
C3309 0.1UF/10V
close to L3301 with in 200 mil
0Ohm R3301 FB12
+AVDD12
C3301 0.1UF/10V
C3302 0.1UF/10V
C3303 0.1UF/10V
C3304 0.1UF/10V
L3303 80Ohm/100Mhz
+EVDD12
C3310 0.1UF/10V
C3311 0.1UF/10V
L3304 80Ohm/100Mhz
LAN_EGND
40mil
+VDD12
C3320 0.1UF/10V
C3321 0.1UF/10V
C3322 0.1UF/10V
C3323 0.1UF/10V
C3324 0.1UF/10V
C3325 0.1UF/10V
XTAL1_LAN
XTAL2_LAN
X3302 25Mhz
C3341 27PF/50V
C3342 27PF/50V
R3310 2.49KOhm
close to pin64
+AVDD33
DSM function note:
At S0 stage, when un-plug LAN cable, the RTLAN_DSM_EN# will pull-low to notice the system, then the system will pull-high the RTLAN_VCC33_EN# to cut off the ISOLATEB pin power.
注意 Pin 65 要多打 via 來散熱
Reserved DSM Function
R3319 0Ohm
RTLAN_DSM# 30
RTLAN_DSM_EN 30
RTLAN_DSM# ---> Check with Bruce
RTLAN_DSM_EN --> Check with Bruce
R3320 3.6KOhm
+3VS
Q3301 2N7002
R3307 1KOhm
R3317 0Ohm
@
ISOLATEB
R3309 15KOhm
@
CLK_LAN_REQ# 29
U3301
RTL8111C_VB_GR
LAN_RSET
LAN_VDDSR
LAN_P51
EESK
EEDI/AUX
EEDO
EECS
T3301
T3302
T3303
VCTRL12
L_TDP
L_TDN
L_RDP
L_RDN
L_TRDP2
L_TRDM2
L_TRDP3
L_TRDM3
FB12
PCIE_WAKE#
PCIE_WAKE#_R
R3321 0Ohm
20,21,43,53 PCIE_WAKE#
PELAN_RST#
+EVDD12
LAN_RST#
R3322 0Ohm
PELAN_RST#
R3306 10KOhm
C3356 0.1UF/10V
+3V
U3304
NC7SZ08P5X
11,21,42 PLT_RST#
R3304 10KOhm
R3323 0Ohm
LAN_EGND
close to LAN CHIP
C3335 0.1UF/10V
C3332 0.1UF/10V
PCIE_RXN1_LAN 21
PCIE_RXP1_LAN 21
CLK_PCIE_LAN# 29
CLK_PCIE_LAN 29
PCIE_TXN1_LAN 21
PCIE_TXP1_LAN 21
40 mil
C3326 0.1UF/10V
C3327 22UF/6.3V
C3328 0.1UF/10V
C3329 0.1UF/10V
R3316 0Ohm
40mil
C3330 0.1UF/10V
C3331 0.1UF/10V
Pin.33 is Clkreq# pin similar to Clkrun function in the PCI interface. If this function not implemented, make this pin floating or connect to the ground.
R3303 0Ohm
@
Q3305 SI3460DV
+12V
R3327 100KOhm
LAN_PWRON
C3354 0.1UF/10V
C3308 22UF/6.3V
R3326 330Ohm
C3312 0.01UF/16V
R3325 220KOhm
+V3.3_LAN_DSG
Q3304 2N7002
R3308 100KOhm
LAN_PWR_ON#
Q3302A UM6K1N
Q3302B UM6K1N
30 LAN_PWR_ON
R3324 100KOhm
ASUSTeK COMPUTER INC
Title : LAN
Engineer: ENGINEER
Size Custom
Project Name N10
Rev 1.0
Date: Wednesday, July 02, 2008
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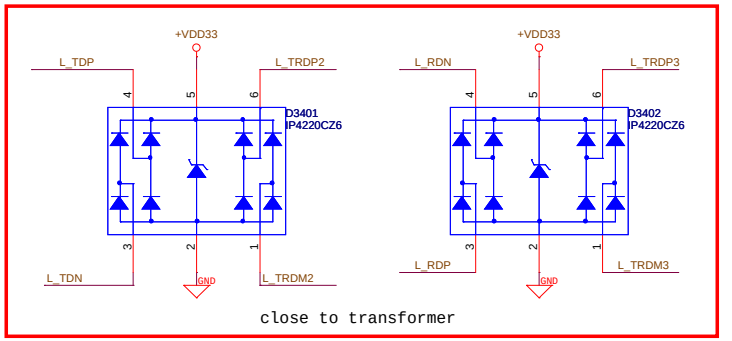
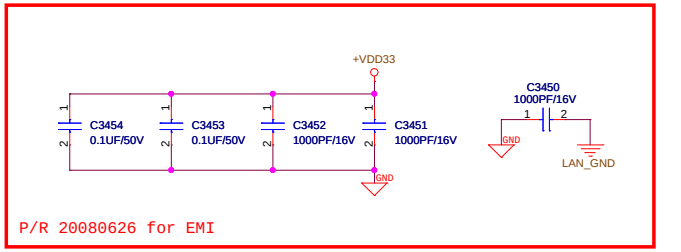
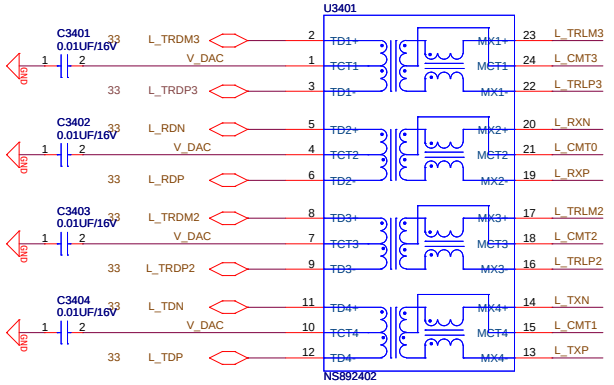
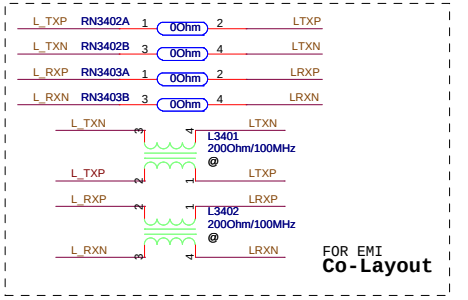
P/R 20080630 SWAP D3401(pin1,pin6) and D3402(pin3,pin4)

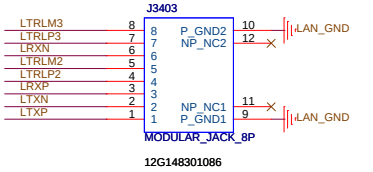


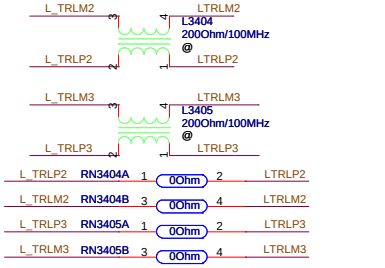


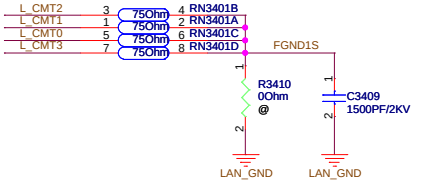


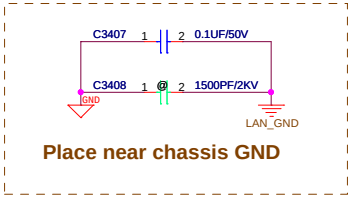
Transformer close to J3401

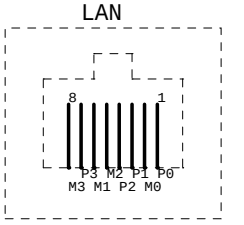












ASUSTeK COMPUTER INC

Title : LAN

Engineer: ENGINEER

Size	Project Name	Rev
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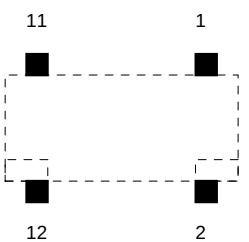
MDC



ASUS	Title : MDC	
ASUSTeK COMPUTER INC	Engineer: ENGINEER	
Size: A	Project Name: N10	Rev: 1.0
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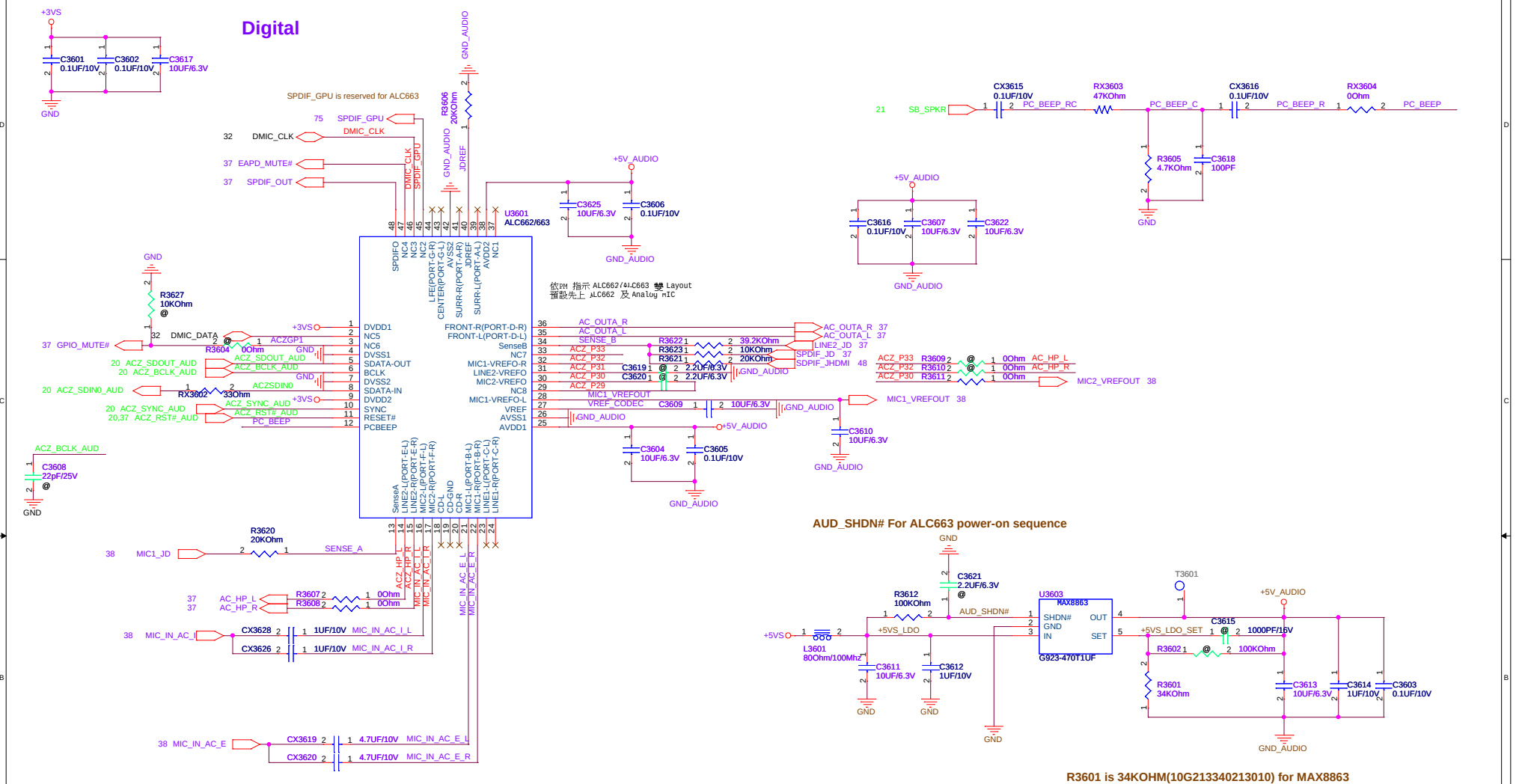
Digital
SPDIF_GPU is reserved for ALC663
U3601
ALC662/663
依PM 指示 ALC662/ALC663 變 Layout
擺設先上 ALC662 及 Analog MIC
AUD_SHDN# For ALC663 power-on sequence
U3603
MAX8863
G923-470T1UF
R3601 is 34KOHM(10G213340213010) for MAX8863
R3601 is 0 OHM(10G213340213010) for GMT923
For EMI
R3613 0Ohm
L3603 120Ohm/100Mhz
L3604 120Ohm/100Mhz
L3605 120Ohm/100Mhz
Title : AUDIO CODEC
ASUSTeK COMPUTER INC
Engineer: ENGINEER
Size Custom
Project Name N10
Rev 1.0
Date: Wednesday, July 02, 2008
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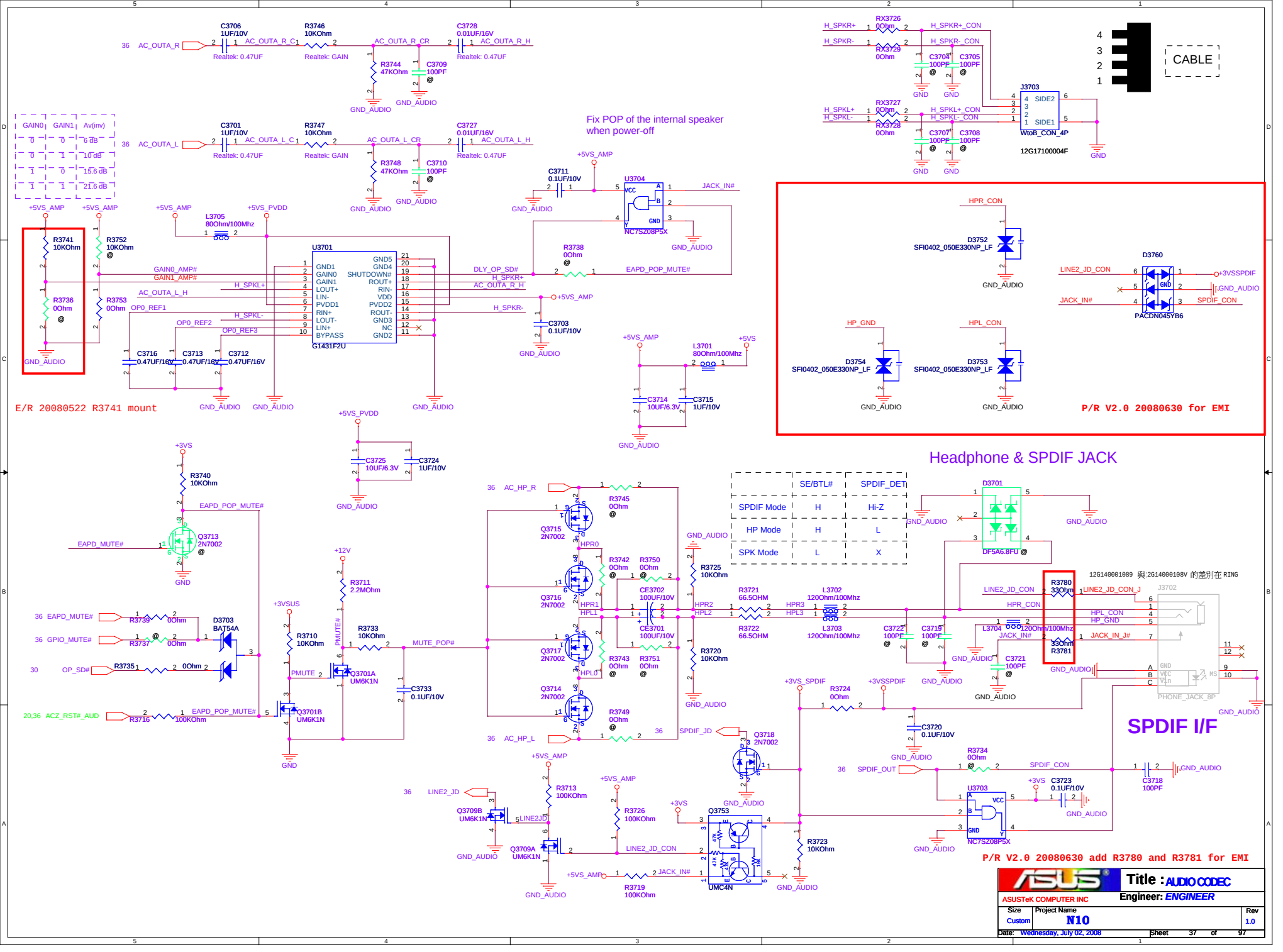
C3706 1UF/10V
R3746 10KOhm
C3728 0.01UF/16V
AC_OUTA_R
AC_OUTA_R_C
AC_OUTA_R_CR
AC_OUTA_R_H
Realtek: 0.47UF
Realtek: GAIN
R3744 47KOhm
C3709 100PF
GND_AUDIO
C3701 1UF/10V
R3747 10KOhm
C3727 0.01UF/16V
AC_OUTA_L
AC_OUTA_L_C
AC_OUTA_L_CR
AC_OUTA_L_H
R3748 47KOhm
C3710 100PF
GAIN0 GAIN1 Av(inv)
0 0 6 dB
0 1 10 dB
1 0 15.6 dB
1 1 21.6 dB
Fix POP of the internal speaker when power-off
C3711 0.1UF/10V
U3704
VCC
GND
NC7SZ08P5X
JACK_IN#
R3738 0Ohm
EAPD_POP_MUTE#
+5VS_AMP
+5VS_PVDD
L3705 80Ohm/100Mhz
R3741 10KOhm
R3752 10KOhm
R3736 0Ohm
R3753 0Ohm
U3701
GND1
GAIN0
GAIN1
LOUT+
LIN-
PVDD1
RIN+
LOUT-
LIN+
BYPASS
GND5
GND4
SHUTDOWN#
ROUT+
RIN-
VDD
PVDD2
ROUT-
GND3
NC
GND2
G1431F2U
GAIN0_AMP#
GAIN1_AMP#
H_SPKL+
AC_OUTA_L_H
OP0_REF1
H_SPKL-
OP0_REF2
OP0_REF3
DLY_OP_SD#
H_SPKR+
AC_OUTA_R_H
H_SPKR-
C3703 0.1UF/10V
C3716 0.47UF/16V
C3713 0.47UF/16V
C3712 0.47UF/16V
E/R 20080522 R3741 mount
L3701 80Ohm/100Mhz
+5VS
C3714 10UF/6.3V
C3715 1UF/10V
C3725 10UF/6.3V
C3724 1UF/10V
+3VS
R3740 10KOhm
Q3713 2N7002
EAPD_MUTE#
GND
+12V
R3711 2.2MOhm
R3710 10KOhm
R3733 10KOhm
MUTE_POP#
PMUTE
PMUTE#
Q3701A UM6K1N
Q3701B UM6K1N
C3733 0.1UF/10V
R3739 0Ohm
R3737 0Ohm
D3703 BAT54A
R3735 0Ohm
OP_SD#
R3716 100KOhm
ACZ_RST#_AUD
AC_HP_R
AC_HP_L
R3745 0Ohm
Q3715 2N7002
Q3716 2N7002
Q3717 2N7002
Q3714 2N7002
HPR0
HPL0
R3742 0Ohm
R3750 0Ohm
CE3702 100UF/10V
CE3701 100UF/10V
R3743 0Ohm
R3751 0Ohm
R3749 0Ohm
R3725 10KOhm
R3720 10KOhm
HPR1
HPL1
HPR2
HPL2
R3721 66.5OHM
R3722 66.5OHM
L3702 120Ohm/100Mhz
L3703 120Ohm/100Mhz
HPR3
HPL3
SE/BTL# SPDIF_DET
SPDIF Mode H Hi-Z
HP Mode H L
SPK Mode L X
SPDIF_JD
Q3718 2N7002
LINE2_JD
Q3709B UM6K1N
Q3709A UM6K1N
LINE2JD
R3713 100KOhm
R3726 100KOhm
LINE2_JD_CON
R3719 100KOhm
Q3753
UMC4N
R3723 10KOhm
+3VS_SPDIF
R3724 0Ohm
+3VSSPDIF
C3720 0.1UF/10V
R3734 0Ohm
SPDIF_OUT
SPDIF_CON
C3723 0.1UF/10V
C3718 100PF
U3703
NC7SZ08P5X
Headphone & SPDIF JACK
D3701
DF5A6.8FU
LINE2_JD_CON
HPR_CON
HPL_CON
HP_GND
JACK_IN_J#
R3780 33Ohm
R3781 33Ohm
L3704 120Ohm/100Mhz
C3721 100PF
C3722 100PF
C3715 100PF
12G140001089 與 2G14000108V 的差別在 RING
J3702
PHONE_JACK_8P
SPDIF I/F
P/R V2.0 20080630 add R3780 and R3781 for EMI
RX3726 0Ohm
RX3729 0Ohm
RX3727 0Ohm
RX3728 0Ohm
H_SPKR+
H_SPKR-
H_SPKR+_CON
H_SPKR-_CON
H_SPKL+
H_SPKL-
H_SPKL+_CON
H_SPKL-_CON
C3704 100PF
C3705 100PF
C3707 100PF
C3708 100PF
J3703
SIDE2
SIDE1
WtoB_CON_4P
12G17100004F
CABLE
HPR_CON
D3752 SFI0402_050E330NP_LF
LINE2_JD_CON
JACK_IN#
D3760
PACDN045YB6
+3VSSPDIF
SPDIF_CON
HP_GND
D3754 SFI0402_050E330NP_LF
HPL_CON
D3753 SFI0402_050E330NP_LF
P/R V2.0 20080630 for EMI
Title : AUDIO CODEC
ASUSTeK COMPUTER INC
Engineer: ENGINEER
Size Custom
Project Name N10
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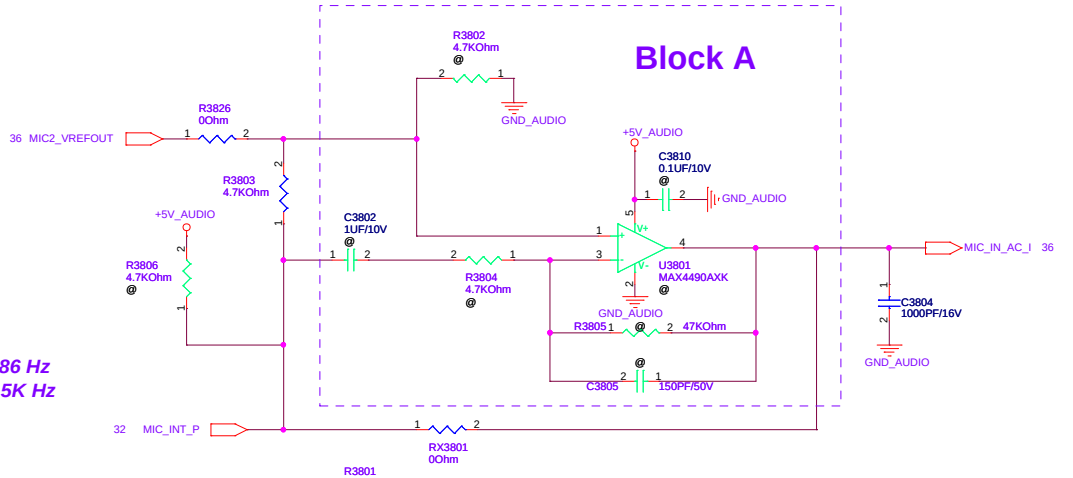
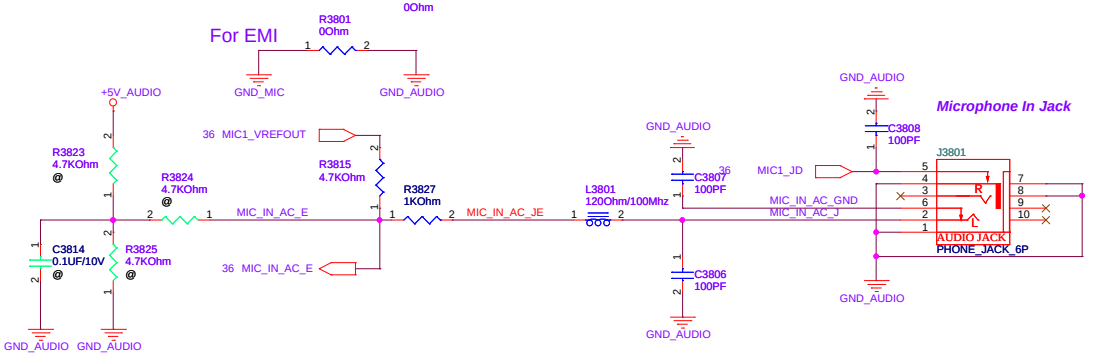
Internal MIC Pre-Amplifier



(Microphone)FL = 33.86 Hz
(Microphone)FH = 22.5K Hz

External MIC



ASUSTeK COMPUTER INC	Title : MICROPHONE	
	Engineer: ENGINEER	
Size: Custom	Project Name: N10	Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 38 of 97	

ASUSTeK COMPUTER INC	Title : EMPTY		
	Engineer: ENGINEER		
Size: A	Project Name: N10		Rev: 1.0
Date: Wednesday, July 02, 2008		Sheet 39 of 97	

ASUSTeK COMPUTER INC	Title : EMPTY	
	Engineer: ENGINEER	
Size: A	Project Name: N10	Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 40 of 97	

ASUSTeK COMPUTER INC	Title : EMPTY		
	Engineer: ENGINEER		
Size: A	Project Name: N10		Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 41 of 97		

xD Pin-assignment

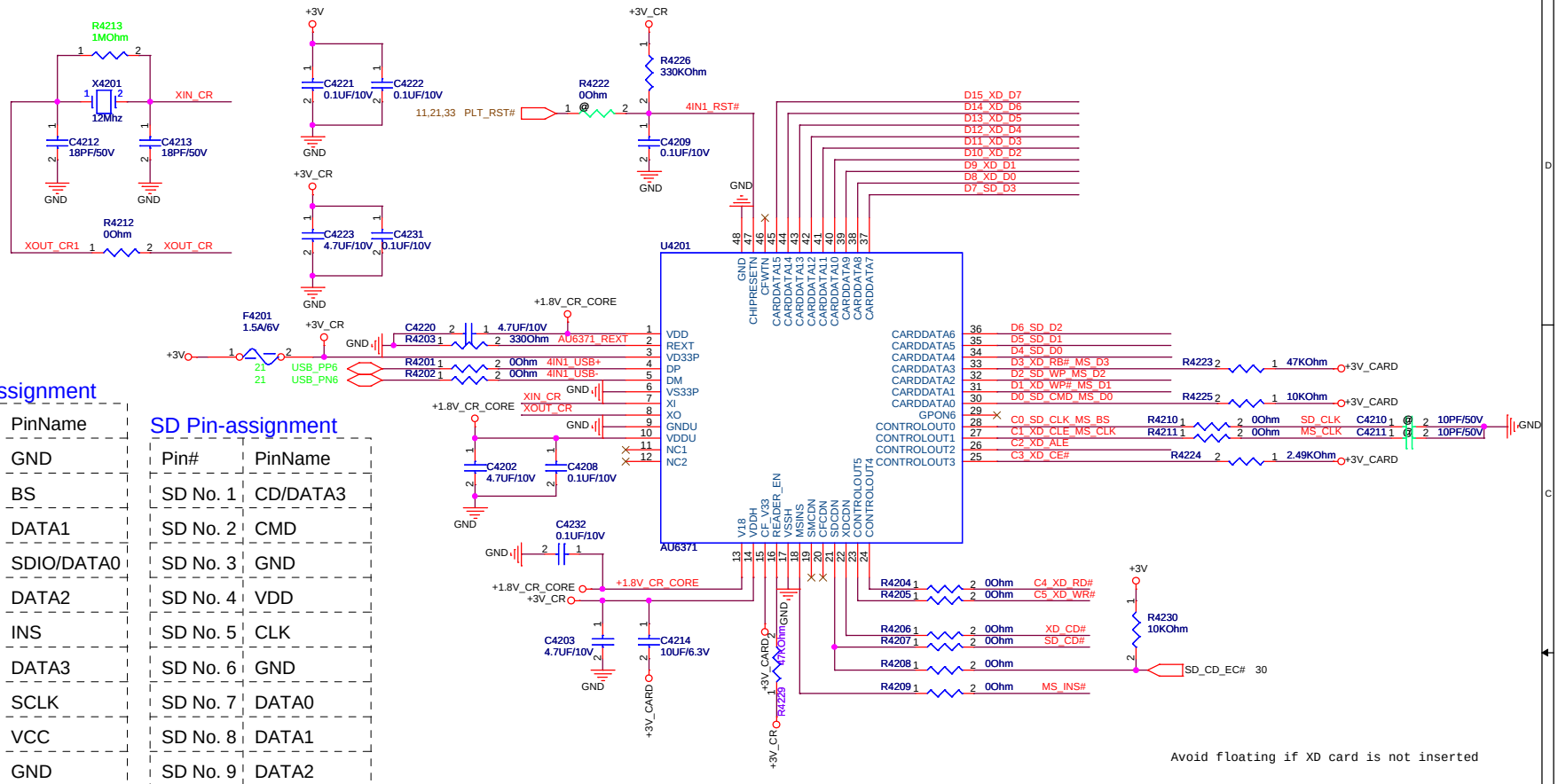
Pin#	PinName
Xd No. 0	CD
Xd No. 1	GND
Xd No. 2	R/-B
Xd No. 3	-RE
Xd No. 4	-CE
Xd No. 5	CLE
Xd No. 6	ALE
Xd No. 7	-WE
Xd No. 8	-WP
Xd No. 9	GND
Xd No.10	D0
Xd No.11	D1
Xd No.12	D2
Xd No.13	D3
Xd No.14	D4
Xd No.15	D5
Xd No.16	D6
Xd No.17	D7
Xd No.18	VCC

MS Pin-assignment

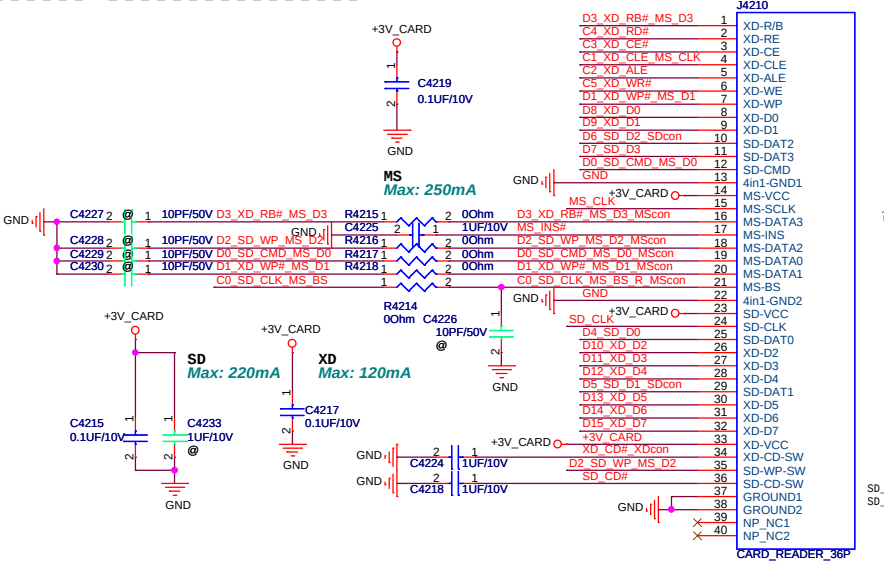
Pin#	PinName
MS No. 1	GND
MS No. 2	BS
MS No. 3	DATA1
MS No. 4	SDIO/DATA0
MS No. 5	DATA2
MS No. 6	INS
MS No. 7	DATA3
MS No. 8	SCLK
MS No. 9	VCC
MS No.10	GND

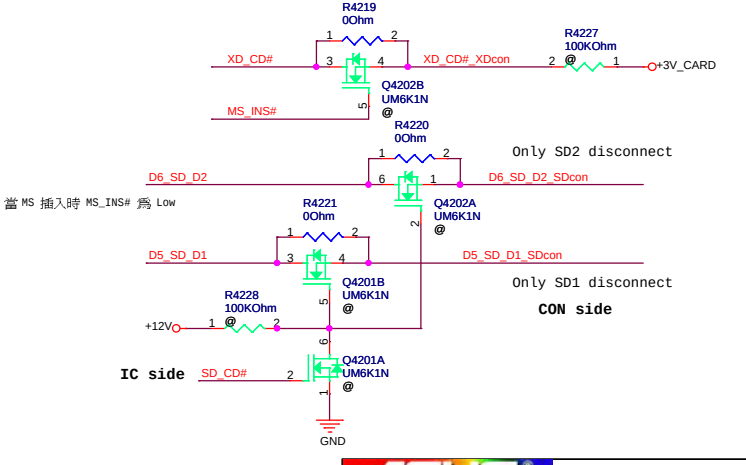
SD Pin-assignment

Pin#	PinName
SD No. 1	CD/DATA3
SD No. 2	CMD
SD No. 3	GND
SD No. 4	VDD
SD No. 5	CLK
SD No. 6	GND
SD No. 7	DATA0
SD No. 8	DATA1
SD No. 9	DATA2



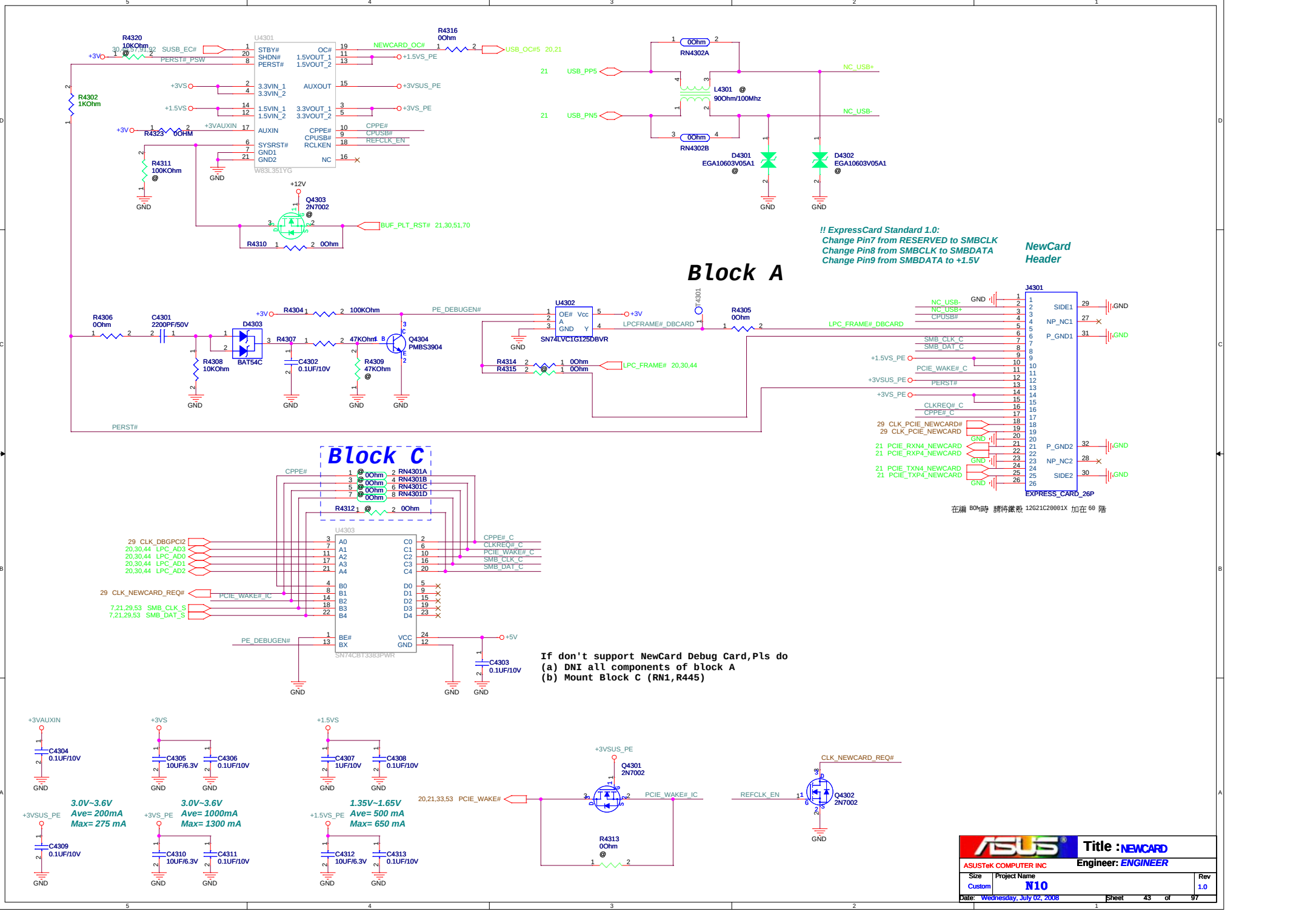
Avoid floating if XD card is not inserted





SD_WP 對於台端連接器是 High 防寫，接地可寫
SD_WP 對於AU6371 是固定無法可程式化

ASUSTeK COMPUTER INC	Title : 4IN1 CARD		
	Engineer: ENGINEER		
Size: Custom	Project Name: N10		Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 42 of 97		


Block A
Block C
NewCard Header
!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V
U4301
W83L351YG
U4302
SN74LVC1G125DBVR
U4303
SN74CBT3383PWR
J4301
EXPRESS_CARD_26P
Q4303 2N7002
Q4304 PMBS3904
Q4301 2N7002
Q4302 2N7002
D4301 EGA10603V05A1
D4302 EGA10603V05A1
L4301 @ 90Ohm/100Mhz
RN4302A
RN4302B
RN4301A
RN4301B
RN4301C
RN4301D
D4303 BAT54C
R4320 10KOhm
R4316 0Ohm
R4302 1KOhm
R4323 0OHM
R4311 100KOhm @
R4310 0Ohm
R4306 0Ohm
C4301 2200PF/50V
R4308 10KOhm
R4304 100KOhm
R4307 47KOhm
C4302 0.1UF/10V
R4309 47KOhm @
R4314 0Ohm
R4315 0Ohm
R4305 0Ohm
R4312 0Ohm
C4303 0.1UF/10V
C4304 0.1UF/10V
C4305 10UF/6.3V
C4306 0.1UF/10V
C4307 1UF/10V
C4308 0.1UF/10V
C4309 0.1UF/10V
C4310 10UF/6.3V
C4311 0.1UF/10V
C4312 10UF/6.3V
C4313 0.1UF/10V
R4313 0Ohm @
3.0V~3.6V
Ave= 200mA
Max= 275 mA
3.0V~3.6V
Ave= 1000mA
Max= 1300 mA
1.35V~1.65V
Ave= 500 mA
Max= 650 mA
If don't support NewCard Debug Card,Pls do
(a) DNI all components of block A
(b) Mount Block C (RN1,R445)
在編 BOM時 請將鐵殼 12G21C20001X 加在 60 階
Title : NEWCARD
ASUSTeK COMPUTER INC
Engineer: ENGINEER
Size Custom
Project Name N10
Rev 1.0
Date: Wednesday, July 02, 2008
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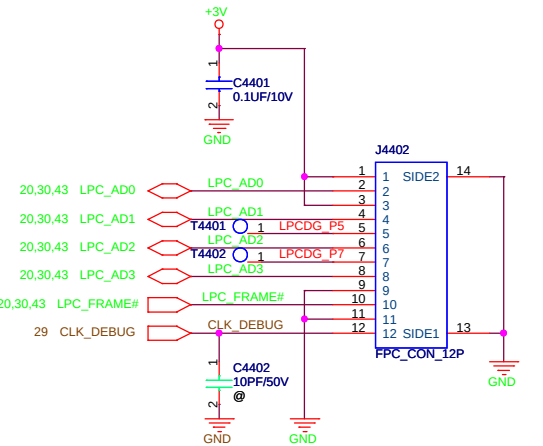
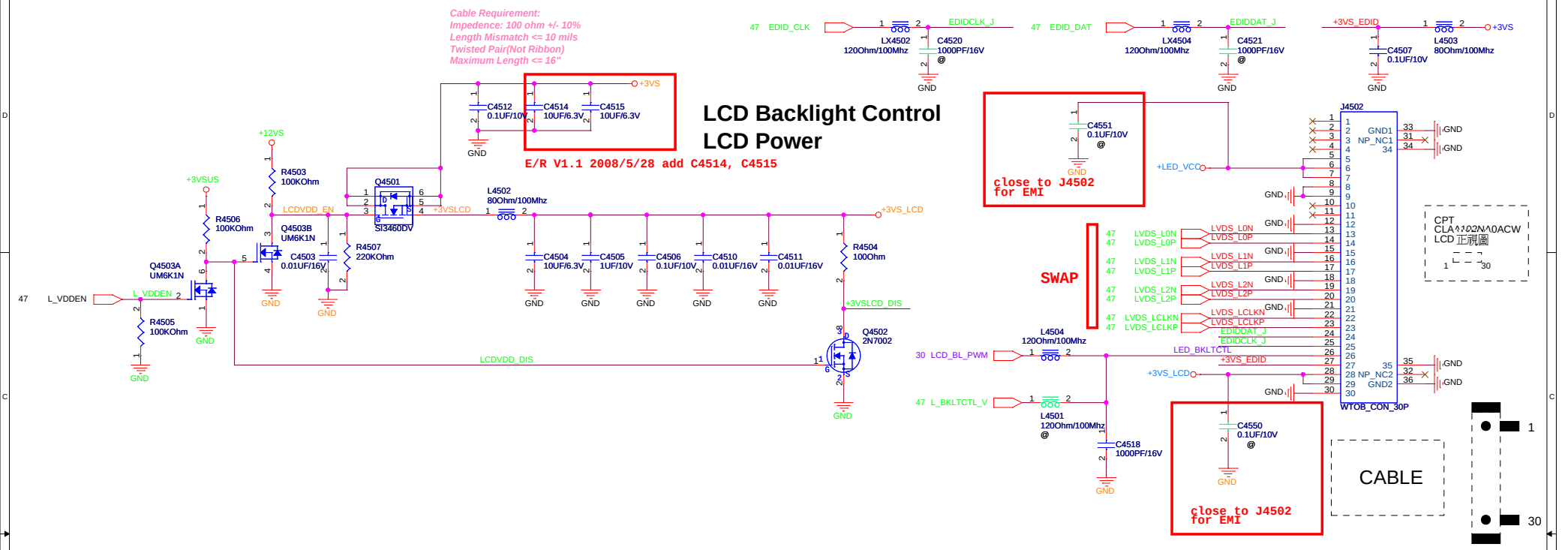
LPC DEBUG PORT



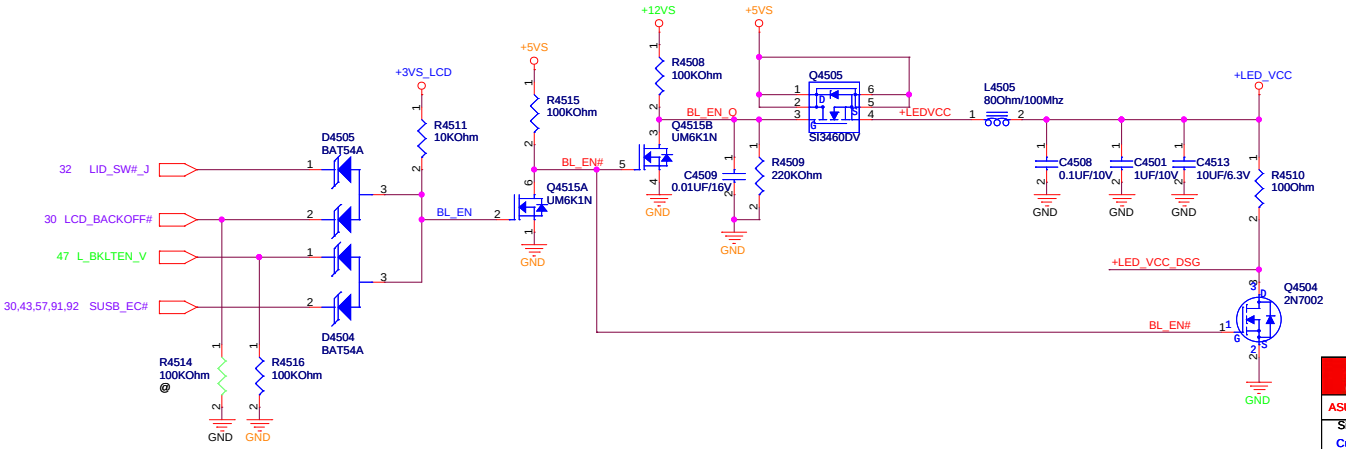
ASUSTeK COMPUTER INC	Title : LPC DEBUG	
	Engineer: ENGINEER	
Size B	Project Name N10	Rev 1.0
Date: Wednesday, July 02, 2008	Sheet 44 of 97	

LCD LVDS Interface



Backlight Interface

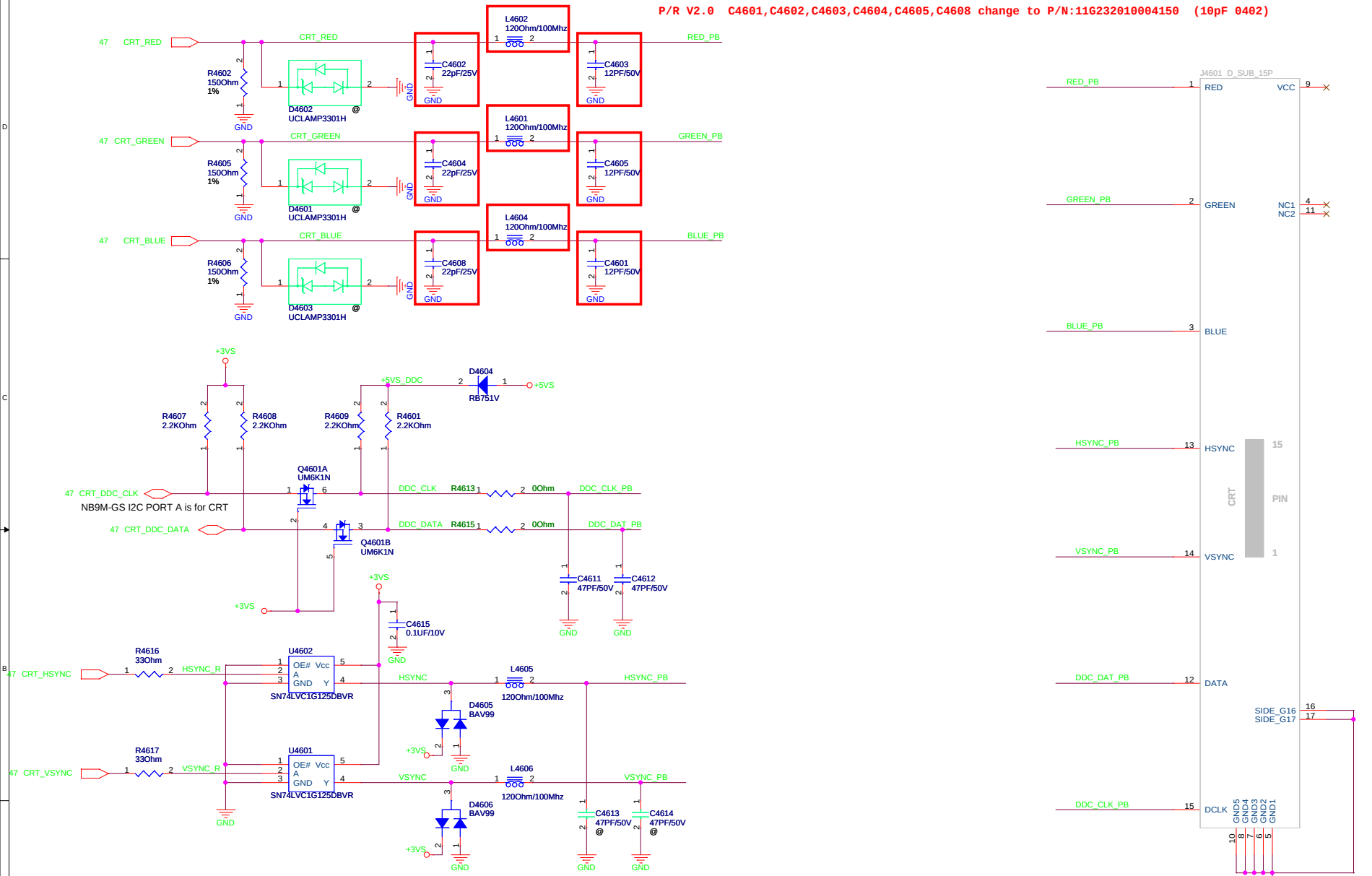
BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.



ASUSTeK COMPUTER INC	Title : LVDS & INVERTER		
	Engineer: ENGINEER		
Size: Custom	Project Name: N10		Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 45 of 97		

P/R V2.0 L4601,L4602,L4604 change to P/N:09G023681002 (0.068UH/300mA 0603 5%)

P/R V2.0 C4601,C4602,C4603,C4604,C4605,C4608 change to P/N:11G232010004150 (10pF 0402)

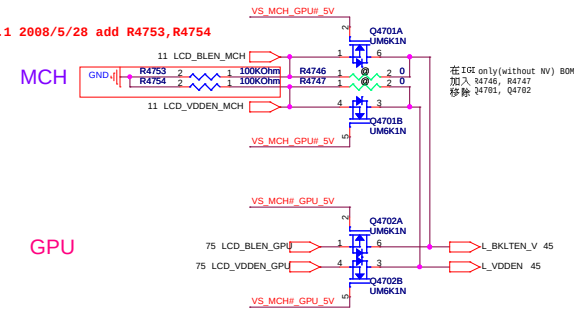


Unidirectional buffers (high impedance buffers) are required on both HSYNC and VSYNC to prevent potential electrical overstress and illegal operation of the GMCH, since some display monitors may attempt to drive HSYNC and VSYNC signals back to GMCH.

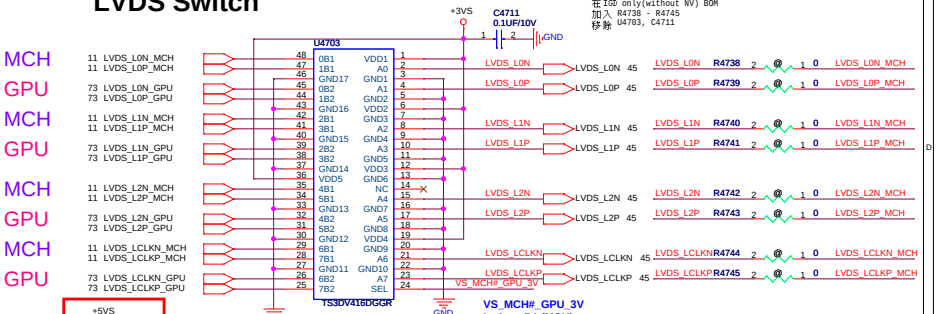
ASUS	Title : CRT	
ASUSTek COMPUTER INC	Engineer: ENGINEER	
Size: Custom	Project Name: N10	Rev: 1.0
Date: Monday, July 07, 2008	Sheet 46 of 97	

LCD/BL Enable Switch

E/R V1.1 2008/5/28 add R4753,R4754



LVDS Switch

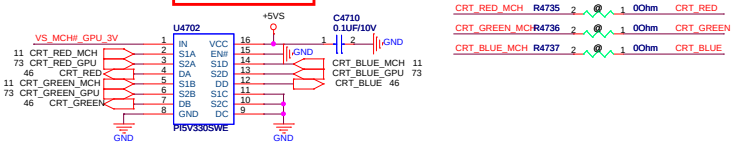


E/R V1.1 2008/5/28 add C4715

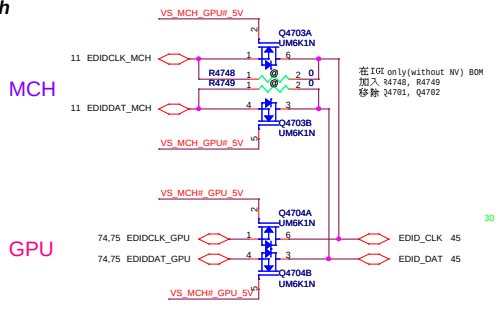
E/R V1.1 2008/5/28 add C4713, C4714

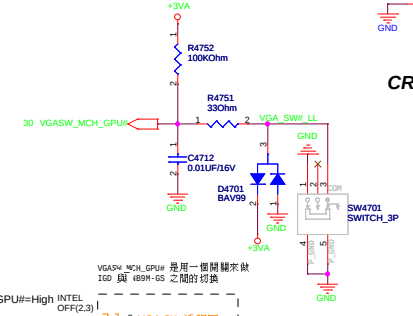
CRT RGB Switch

DAC_SEL
L: Dx=S1x (MCH)
H: Dx=S2x (GPU)

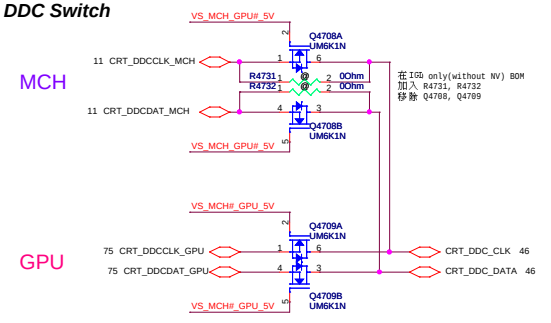


EDID Switch

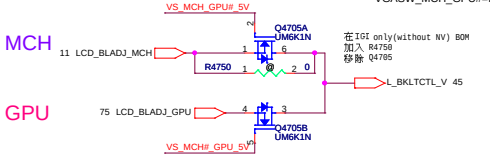


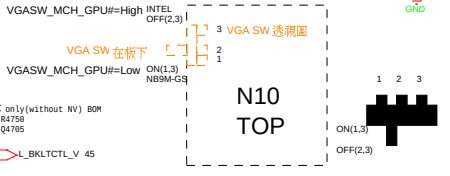


CRT DDC Switch

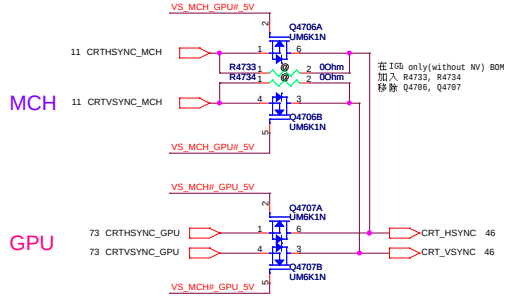


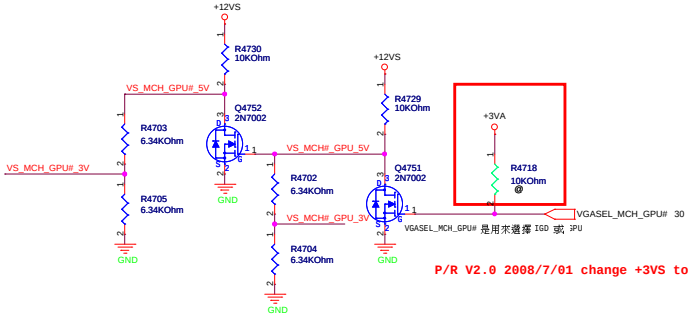
BL PWM Switch





CRT SYNC Switch





P/R V2.0 2008/7/01 change +3VS to +3VA, umount R4718

ASUS / ASUSTeK COMPUTER INC. NB1	Title : Hybrid-Switch	
	Engineer: C.W._Lin	
Size: Custom	Project Name: H17	Rev: 1.0
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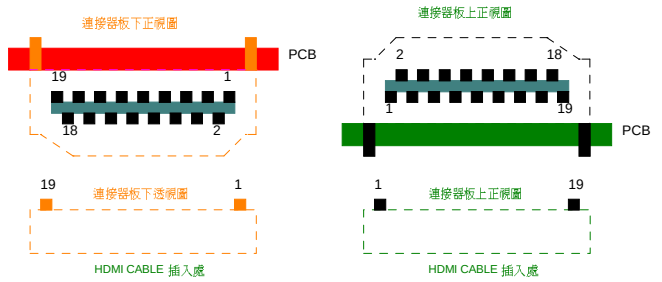
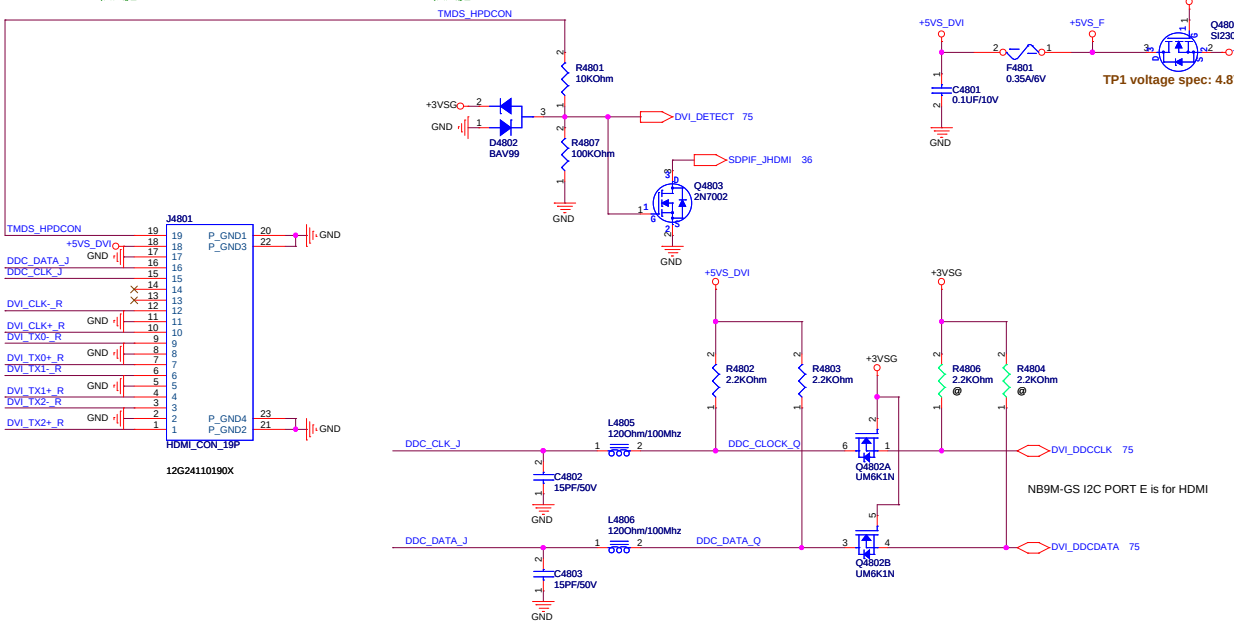
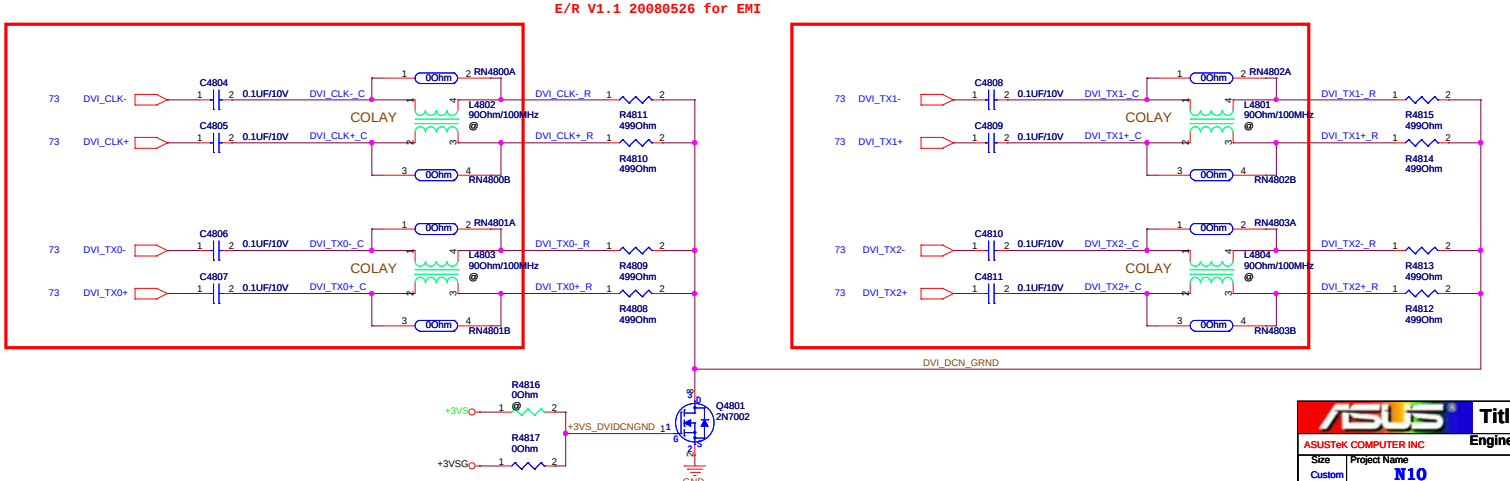




E/R V1.1 20080526 for EMI



ASUS	Title : HDMI	
ASUSTeK COMPUTER INC	Engineer: ENGINEER	
Size: Custom	Project Name: N10	Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 48 of 97	

ASUSTeK COMPUTER INC	Title : EMPTY	
	Engineer: ENGINEER	
Size: A	Project Name: N10	Rev: 1.0
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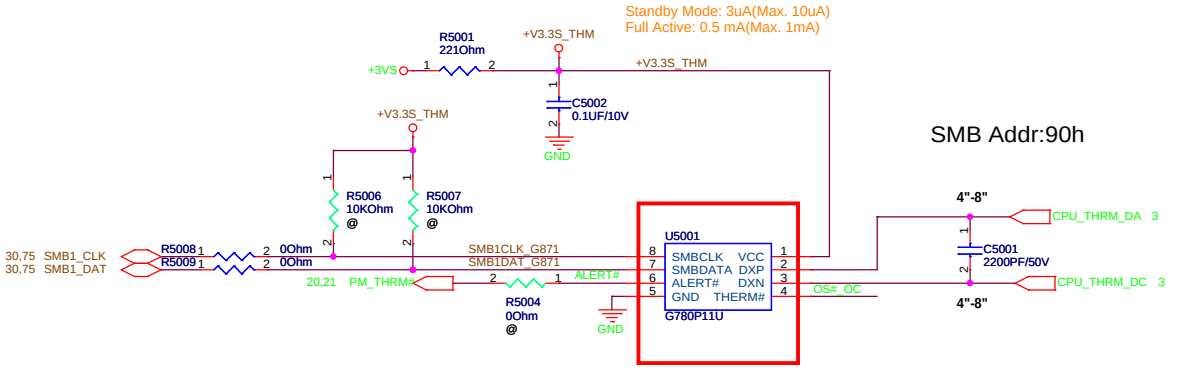
Thermal Sensor



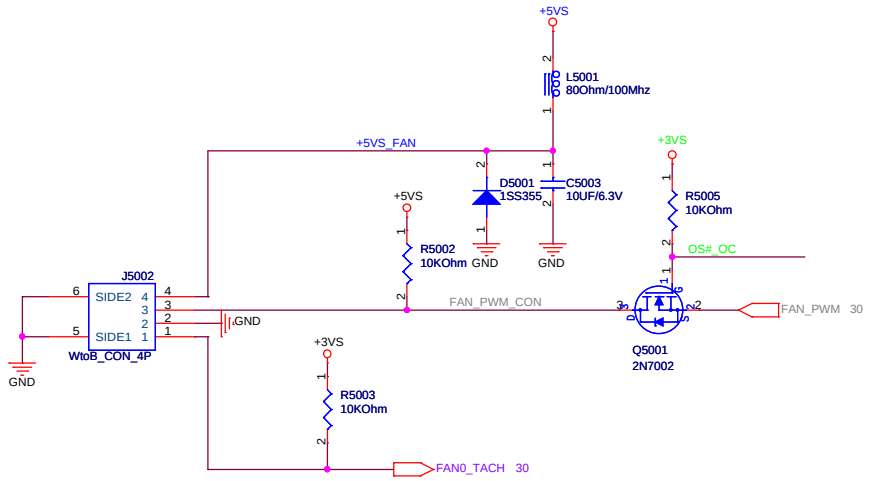
U5001 於3OM變更P/N:06G023064020 E/R 2008/05/19

Route H_THERMDA and H_THERMDC
on the same layer

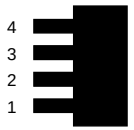
----------OTHER SIGNALS
12 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power

FAN connector



TOP

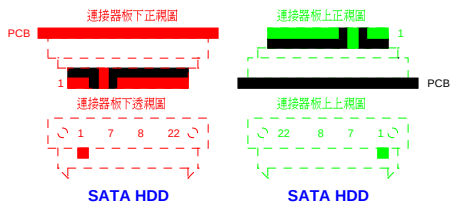


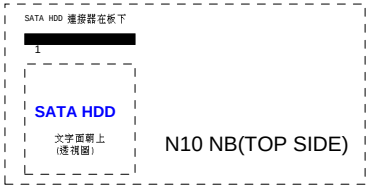
FAN

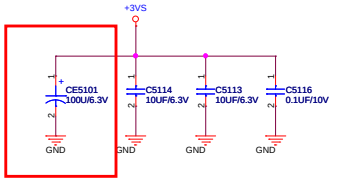
ASUSTeK COMPUTER INC	Title : THER-SENSOR/FAN	
	Engineer: ENGINEER	
Size: Custom	Project Name: N10	Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 50 of 97	

SATA HDD

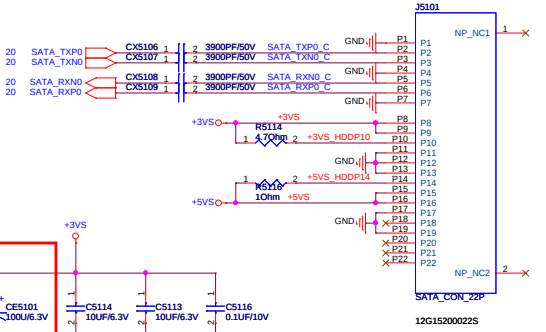
J5101 變更?/N:12G15200022S (DIP)

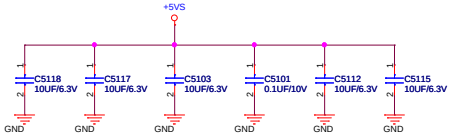






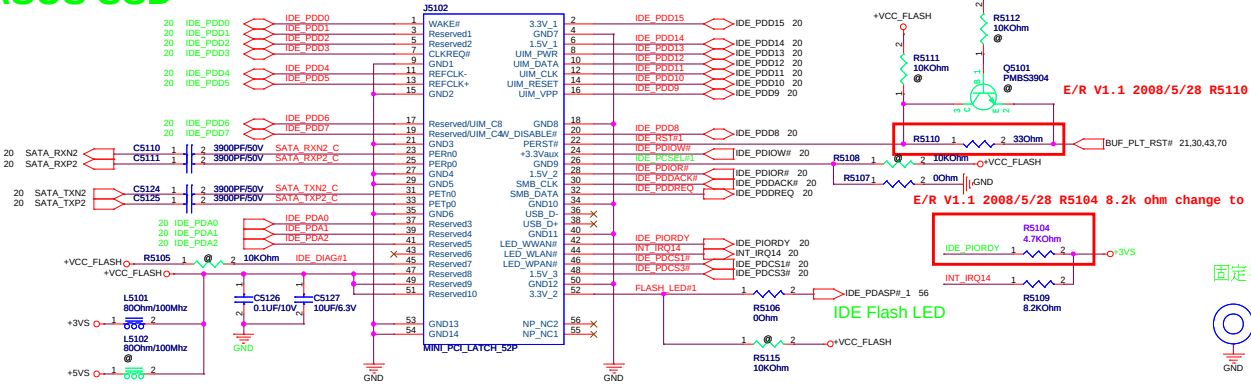
E/R V1.1 2008/5/28 add CE5101





E/R H5103,H5104 Delete

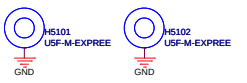
ASUS SSD



E/R V1.1 2008/5/28 R5110 0 ohm change to 33 ohm

E/R V1.1 2008/5/28 R5104 8.2k ohm change to 4.7k ohm

固定 SSD MINICARD 用

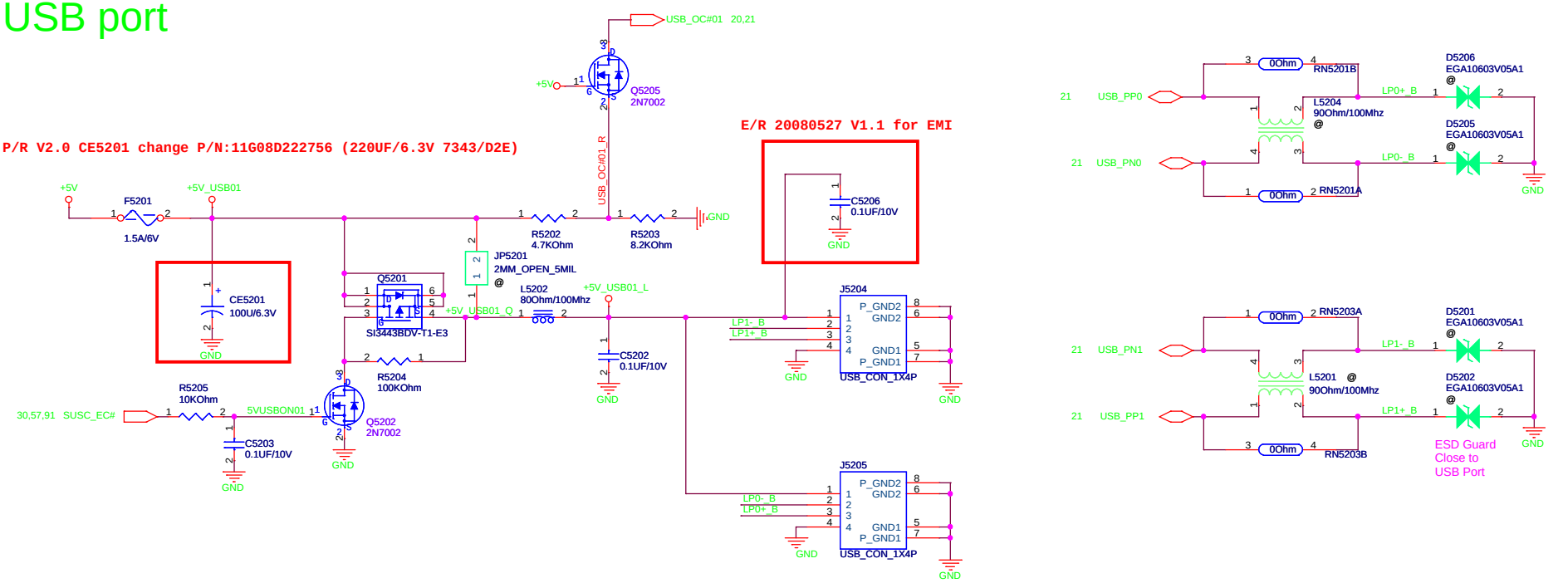


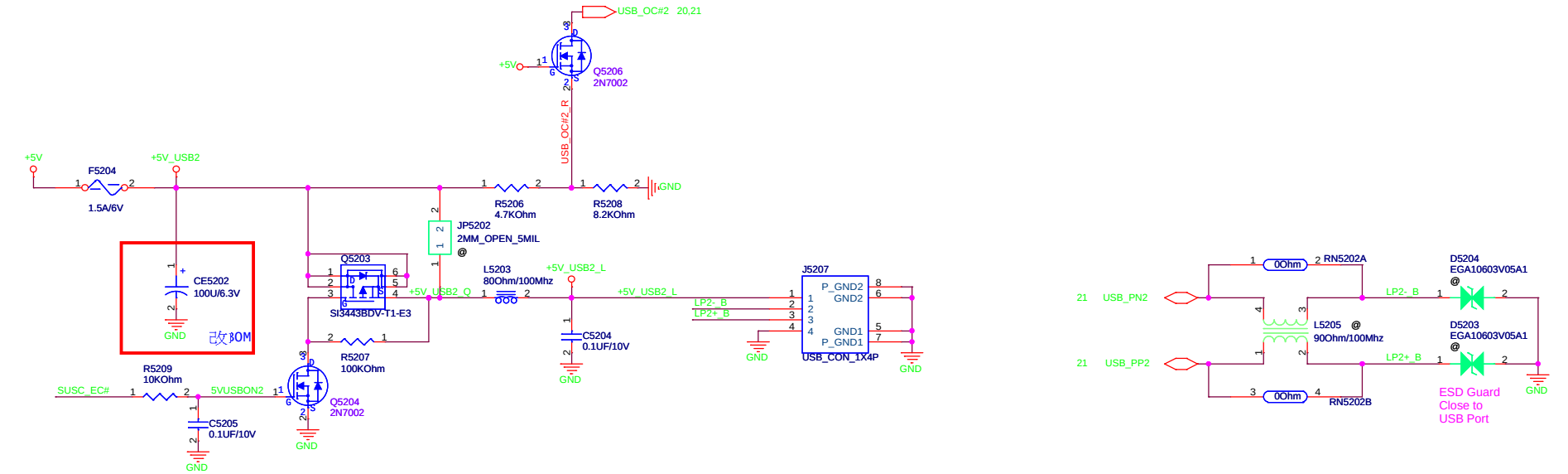
ASUSTeK COMPUTER INC	Title : HDD	Engineer: ENGINEER
Size C	Project Name N10	Rev 1.0
Date: Wednesday, July 02, 2008	Sheet 51 of 97	

USB port

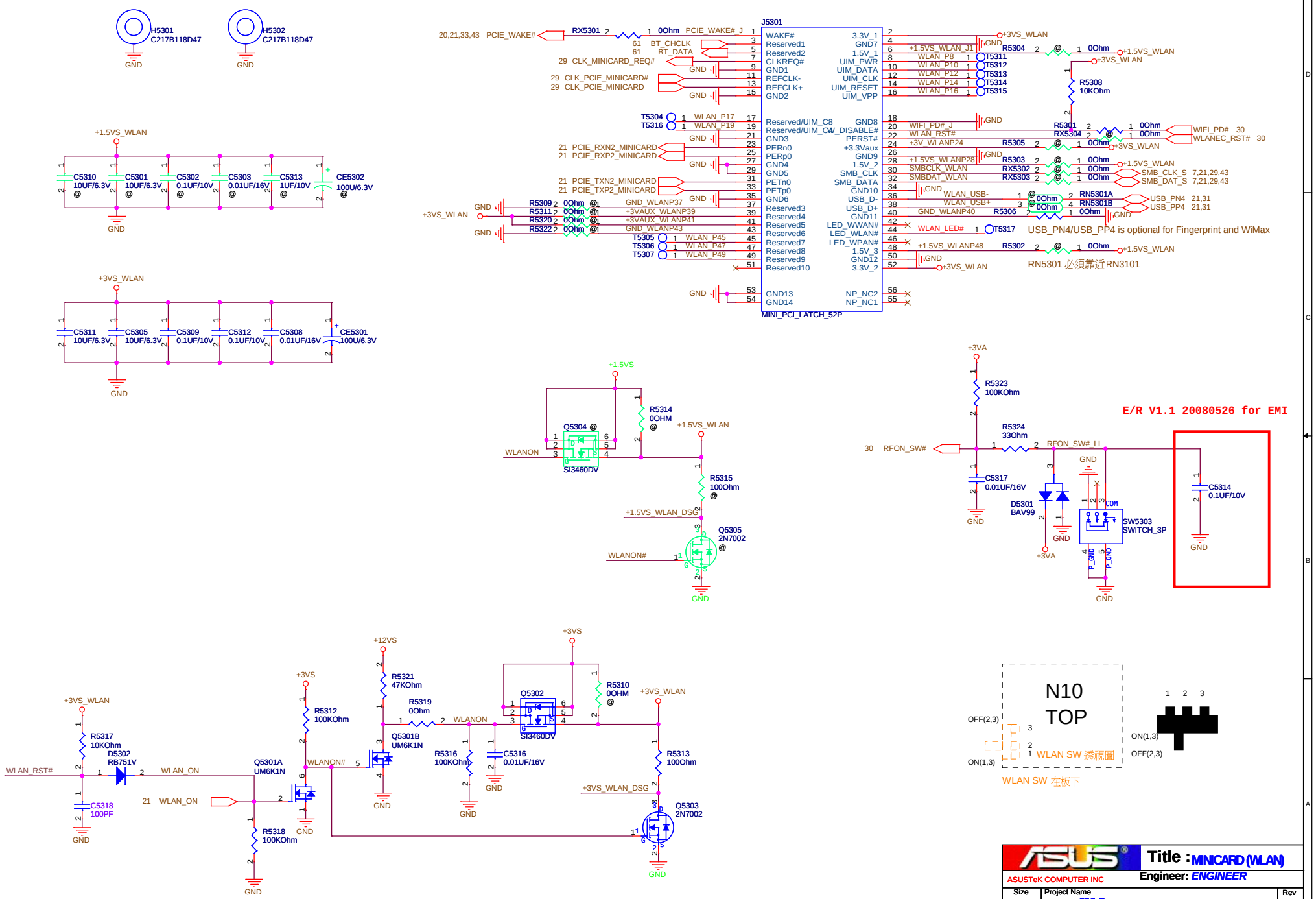
P/R V2.0 CE5201 change P/N:11G08D222756 (220UF/6.3V 7343/D2E)

E/R 20080527 V1.1 for EMI





ASUSTeK COMPUTER INC	Title : USB CONN	
	Engineer: ENGINEER	
Size: Custom	Project Name: N10	Rev: 1.0
Date: Monday, July 07, 2008	Sheet 52 of 97	


H5301 C217B118D47
H5302 C217B118D47
GND
J5301
MINI_PCI_LATCH_52P
20,21,33,43 PCIE_WAKE#
RX5301 0Ohm PCIE_WAKE# J
61 BT_CHCLK
61 BT_DATA
29 CLK_MINICARD_REQ#
29 CLK_PCIE_MINICARD#
29 CLK_PCIE_MINICARD
21 PCIE_RXN2_MINICARD
21 PCIE_RXP2_MINICARD
21 PCIE_TXN2_MINICARD
21 PCIE_TXP2_MINICARD
+3VS_WLAN
R5309 0Ohm GND_WLANP37
R5311 0Ohm +3VAUX_WLANP39
R5320 0Ohm +3VAUX_WLANP41
R5322 0Ohm GND_WLANP43
T5304 WLAN_P17
T5316 WLAN_P19
T5305 WLAN_P45
T5306 WLAN_P47
T5307 WLAN_P49
+1.5VS_WLAN
R5304 0Ohm
R5308 10KOhm
T5311 WLAN_P8
T5312 WLAN_P10
T5313 WLAN_P12
T5314 WLAN_P14
T5315 WLAN_P16
R5301 0Ohm WIFI_PD# 30
RX5304 0Ohm WLANEC_RST# 30
R5305 0Ohm
R5303 0Ohm SMB_CLK_S 7,21,29,43
RX5302 0Ohm SMB_DAT_S 7,21,29,43
RX5303 0Ohm
RN5301A USB_PN4 21,31
RN5301B USB_PP4 21,31
R5306 0Ohm
T5317 WLAN_LED#
USB_PN4/USB_PP4 is optional for Fingerprint and WiMax
R5302 0Ohm
RN5301 必須靠近RN3101
C5310 10UF/6.3V
C5301 10UF/6.3V
C5302 0.1UF/10V
C5303 0.01UF/16V
C5313 1UF/10V
CE5302 100U/6.3V
C5311 10UF/6.3V
C5305 10UF/6.3V
C5309 0.1UF/10V
C5312 0.1UF/10V
C5308 0.01UF/16V
CE5301 100U/6.3V
+1.5VS
R5314 0OHM
Q5304
SI3460DV
WLANON
R5315 100Ohm
+1.5VS_WLAN_DSG
Q5305 2N7002
WLANON#
+3VA
R5323 100KOhm
R5324 33Ohm
30 RFON_SW#
RFON_SW# LL
C5317 0.01UF/16V
D5301 BAV99
SW5303 SWITCH_3P
C5314 0.1UF/10V
E/R V1.1 20080526 for EMI
+12VS
R5321 47KOhm
R5319 0Ohm
Q5301B UM6K1N
R5316 100KOhm
C5316 0.01UF/16V
Q5302
SI3460DV
R5310 0OHM
+3VS
R5312 100KOhm
R5313 100Ohm
+3VS_WLAN_DSG
Q5303 2N7002
WLAN_RST#
R5317 10KOhm
D5302 RB751V
WLAN_ON
21 WLAN_ON
C5318 100PF
Q5301A UM6K1N
WLANON#
R5318 100KOhm
N10
TOP
OFF(2,3)
ON(1,3)
WLAN SW 透視圖
WLAN SW 在板下
1 2 3
ON(1,3)
OFF(2,3)
ASUSTeK COMPUTER INC
Title : MINICARD (WLAN)
Engineer: ENGINEER
Size Custom
Project Name N10
Rev 1.0
Date: Wednesday, July 02, 2008
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Title : EMPTY

ASUSTek COMPUTER INC

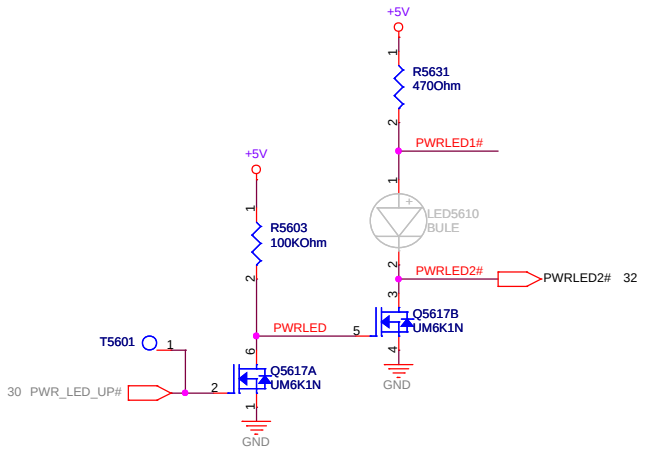
Engineer: ENGINEER

Size	Project Name	Rev
Custom	N10	1.0

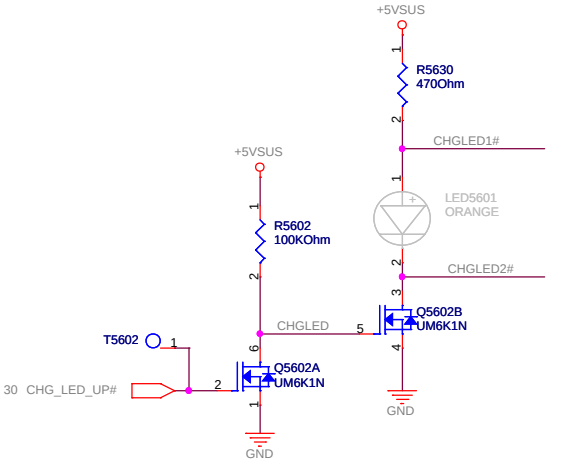
Date: Wednesday, July 02, 2008 Sheet 54 of 97

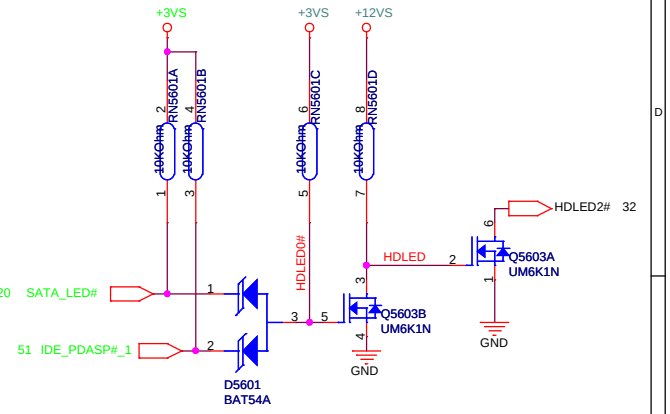
ASUSTeK COMPUTER INC	Title : EMPTY		
	Engineer: ENGINEER		
Size: A	Project Name: N10		Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 55 of 97		

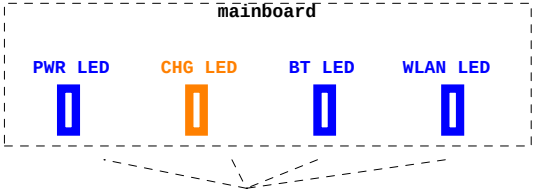
POWER LED



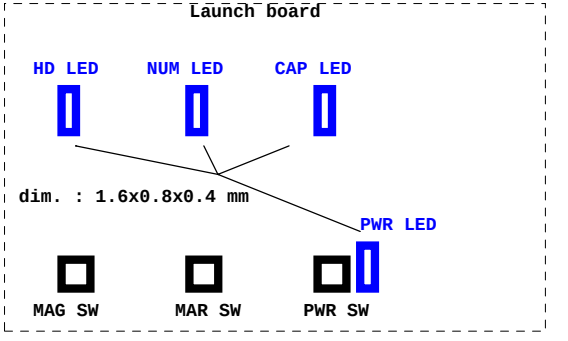
CHARGE LED







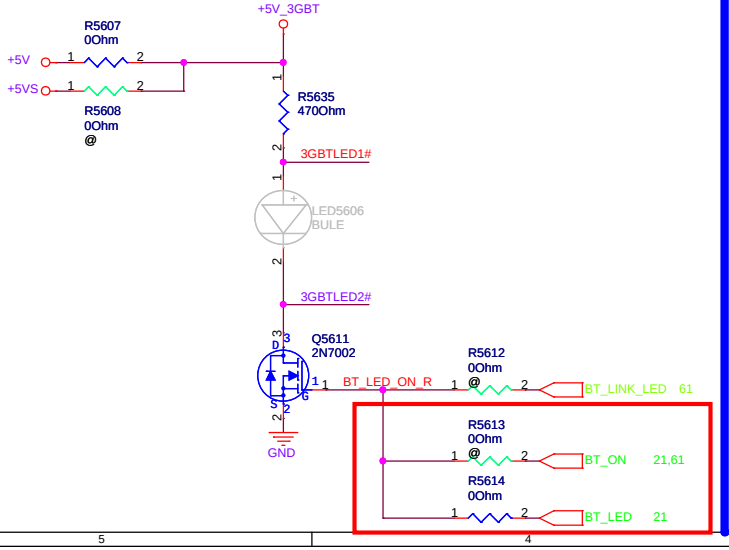
dim. : 3x1.6x1.6 mm



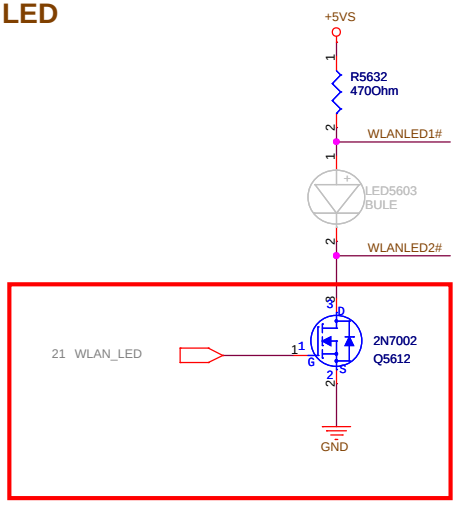
dim. : 1.6x0.8x0.4 mm

BT LED

P/R V2.0 2008/6/29 R5613 unmount, R5614 mount

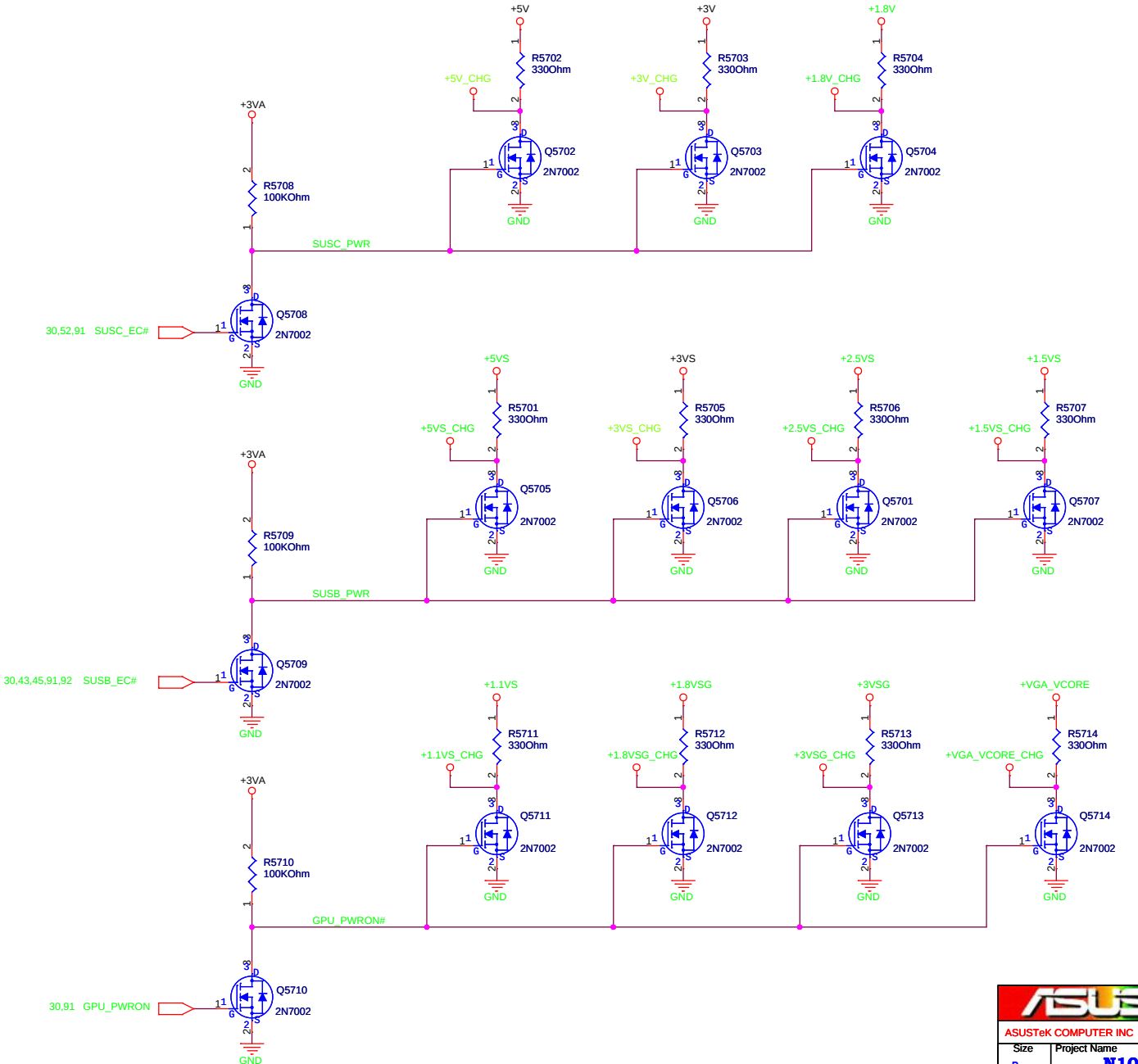


WLAN LED



P/R V2.0 2008/6/29 mount Q5612

ASUS	Title : LED	
ASUSTek COMPUTER INC	Engineer: ENGINEER	
Size B	Project Name N10	Rev 1.0
Date: Wednesday, July 02, 2008	Sheet 56 of 97	



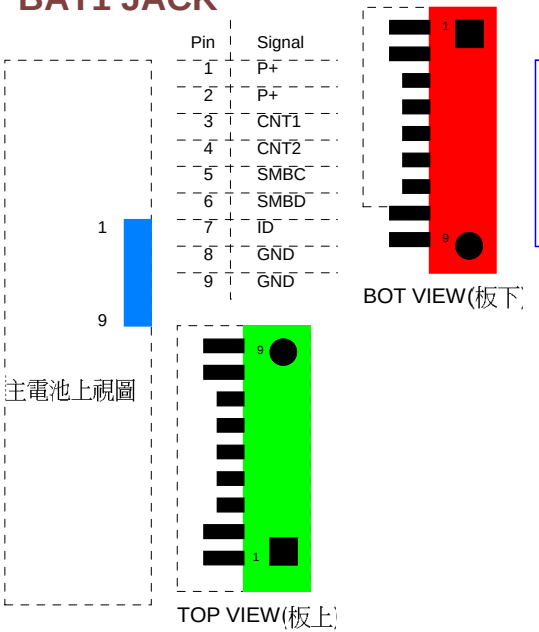
ASUSTeK COMPUTER INC	Title : Discharge Circuit	Engineer: ENGINEER
Size: B	Project Name: N10	Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 57 of 97	

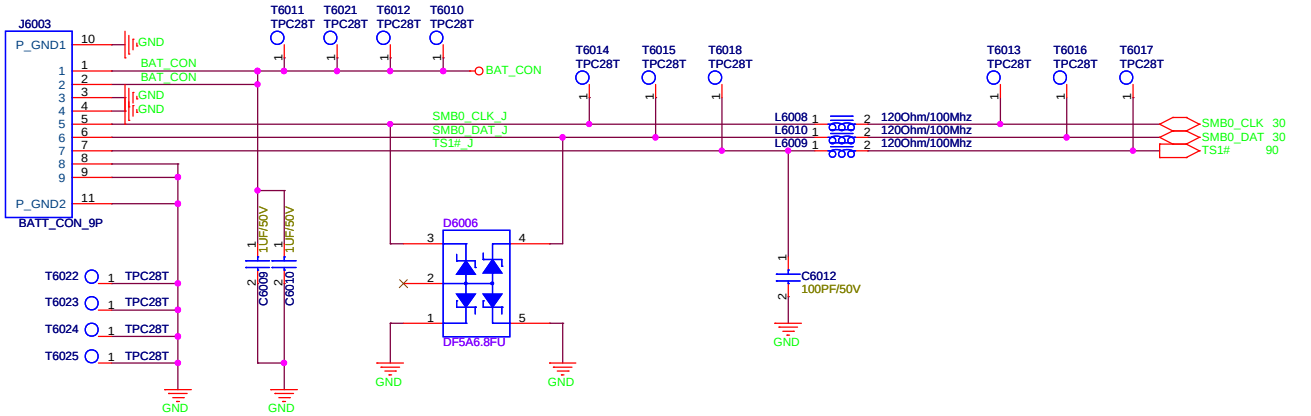
ASUSTeK COMPUTER INC	Title : EMPTY
	Engineer: ENGINEER
Size: B	Project Name: N10
Rev: 1.0	
Date: Wednesday, July 02, 2008	Sheet 58 of 97

ASUSTeK COMPUTER INC	Title : EMPTY
	Engineer: ENGINEER
Size: B	Project Name: N10
Rev: 1.0	
Date: Wednesday, July 02, 2008	Sheet 59 of 97

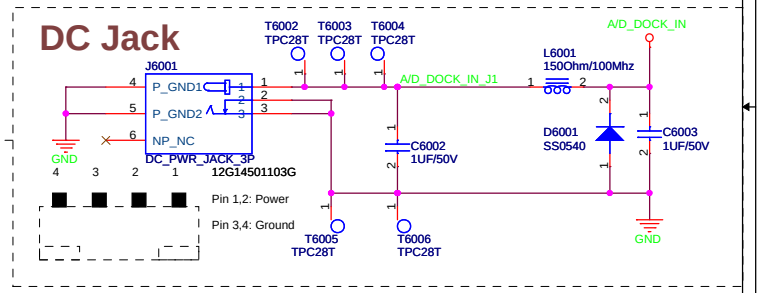
BAT1 JACK

Pin	Signal
1	P+
2	P+
3	CNT1
4	CNT2
5	SMBC
6	SMBD
7	ID
8	GND
9	GND

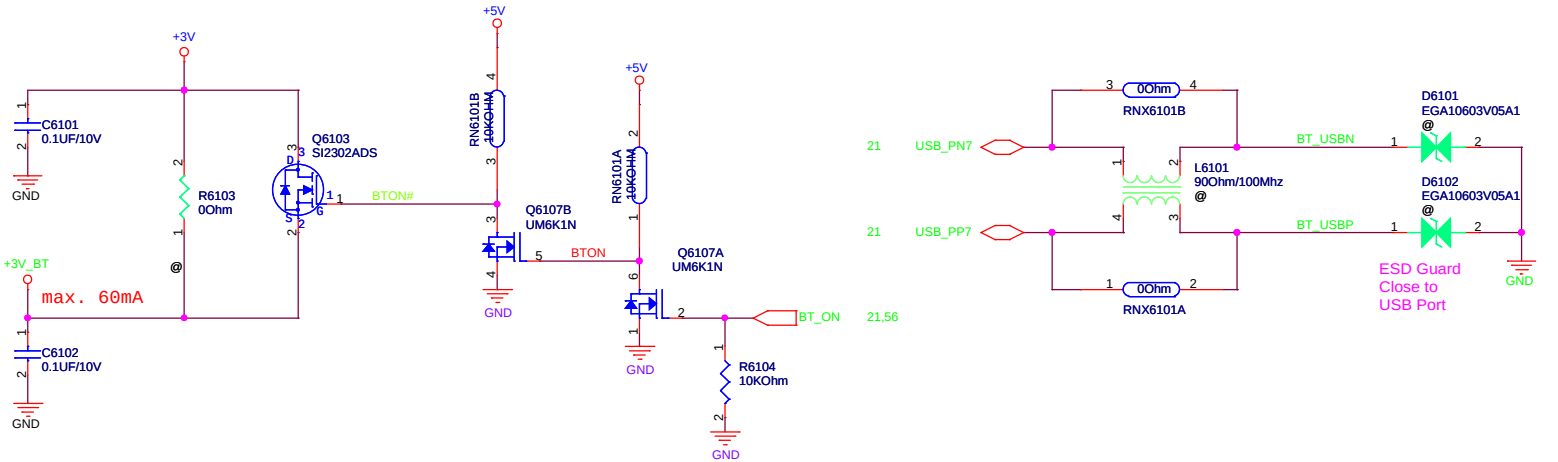


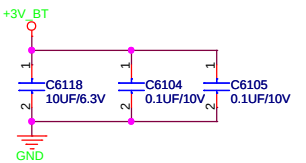


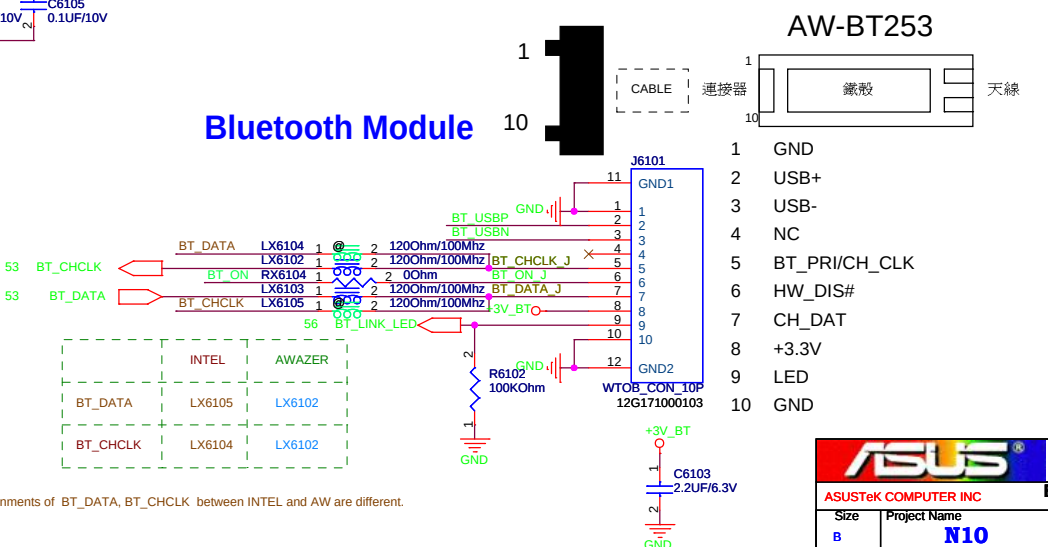
DC Jack



ASUSTeK COMPUTER INC	Title : DC/BATT Conn.	
	Engineer: ENGINEER	
Size: Custom	Project Name: N10	Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 60 of 97	







	INTEL	AWAZER
BT_DATA	LX6105	LX6102
BT_CHCLK	LX6104	LX6102

Pin-assignments of BT_DATA, BT_CHCLK between INTEL and AW are different.

ASUSTeK COMPUTER INC

Title : BLUETOOTH

Engineer: ENGINEER

Size	Project Name	Rev
B	N10	1.0

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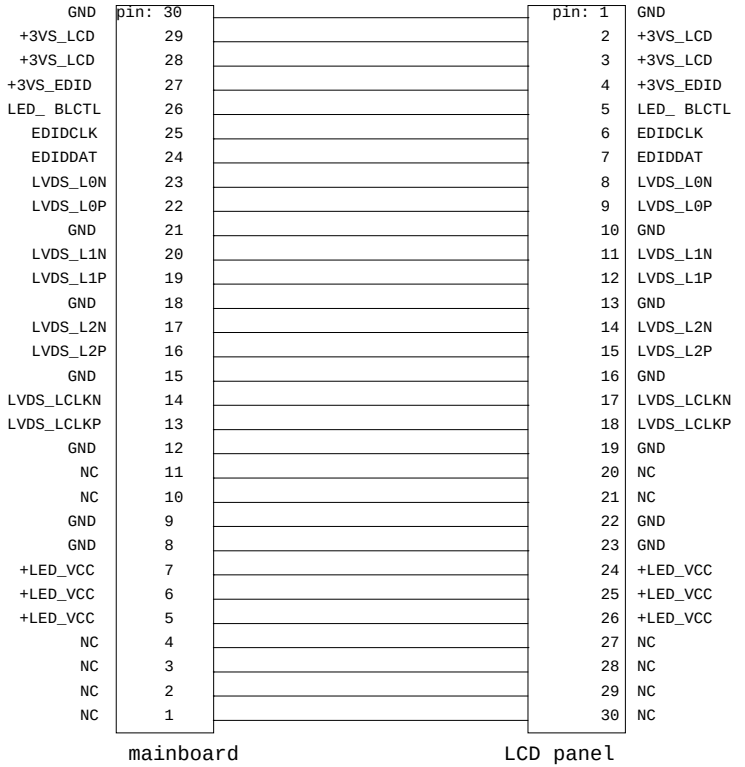

ASUSTeK COMPUTER INC	Title : EMPTY		
	Engineer: ENGINEER		
Size: Custom	Project Name: N10		Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 62 of 97		

ASUSTeK COMPUTER INC	Title : EMPTY		
	Engineer: ENGINEER		
Size: Custom	Project Name: N10		Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 63 of 97		

PCI Device	IDSEL#	REQ/GNT#	Interrupts
Chipset (Host to PCI)	AD30 (Internal)		

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
Thermal Sensor (CPU)	1001100x (98)
Thermal Sensor (VGA)	1001101x (9A)

IC	REFERENCE	VENID	DEVID	VERSION	MARK
NB9M-GS			0x06E9		Current Version: A2

ASUSTeK COMPUTER INC

Title : RESOURCE

Engineer: ENGINEER

Size	Project Name	Rev
Custom	N10	1.0

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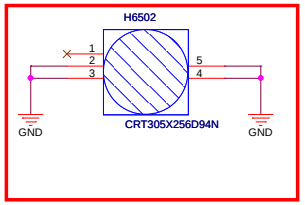
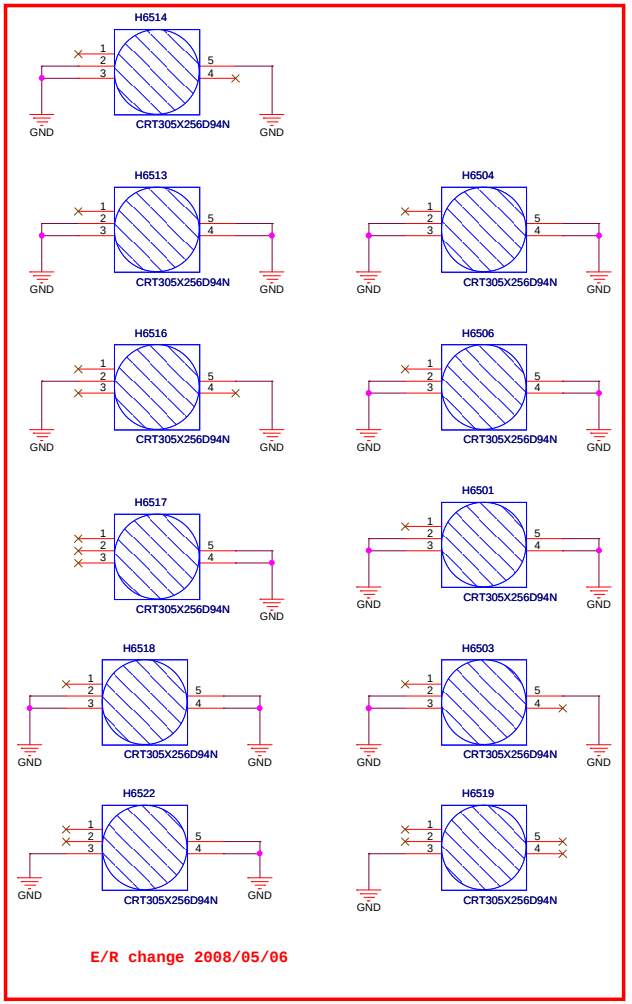
A+E

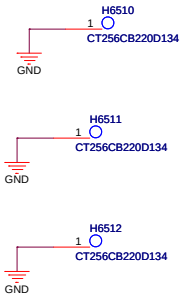


A+B

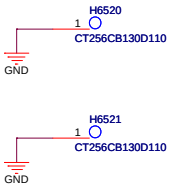


E/R change 2008/05/06

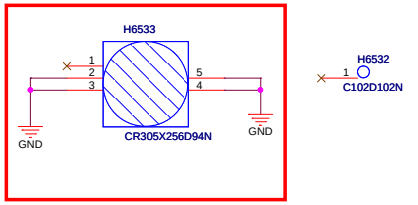
G+H



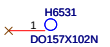
D



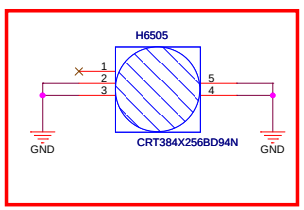
A+A



L



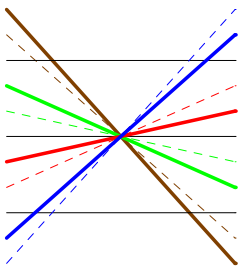
O+B



ASUSTeK COMPUTER INC	Title : ME-SKEWHOLE	
	Engineer: ENGINEER	
Size: Custom	Project Name: N10	Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 65 of 97	

LVDS CABLE (WTB)

	GND	30	1	GND
	+3VS_LCD	29	2	+3VS_LCD
	+3VS_LCD	28	3	+3VS_LCD
	+3VS_EDID	27	4	+3VS_EDID
	LED_BLCTL	26	5	LED_BLCTL
	EDID_CLK	25	6	EDID_CLK
	EDID_DAT	24	7	EDID_DAT
diff. 100ohm	LVDS_LCLKP	23	8	LVDS_L0N
diff. 100ohm	LVDS_LCLKN	22	9	LVDS_L0P
	GND	21	10	GND
diff. 100ohm	LVDS_L2P	20	11	LVDS_L1N
diff. 100ohm	LVDS_L2N	19	12	LVDS_L1P
	GND	18	13	GND
diff. 100ohm	LVDS_L1P	17	14	LVDS_L2N
diff. 100ohm	LVDS_L1N	16	15	LVDS_L2P
	GND	15	16	GND
diff. 100ohm	LVDS_L0P	14	17	LVDS_LCLKN
diff. 100ohm	LVDS_L0N	13	18	LVDS_LCLKP
	GND	12	19	GND
	NC	11	20	NC
	NC	10	21	NC
	GND	9	22	GND
	GND	8	23	GND
	+LED_VCC	7	24	+LED_VCC
	+LED_VCC	6	25	+LED_VCC
	+LED_VCC	5	26	+LED_VCC
	NC	4	27	NC
	NC	3	28	NC
	NC	2	29	NC
	NC	1	30	NC



MAINBOARD CONNECT LCD PANEL CONNECT

P/N: 12G171040305

MIC., CCD, ALS CABLE(WTB)

	GND	1
diff. 90ohm	CCD_USB-	2
diff. 90ohm	CCD_USB+	3
	GND	4
	+5VS_CMOS	5
	+3VS	6
	ALS_AD	7
	GND	8
	INTMIC_A_GND_CON	9
	INTMIC_A_CON	10
	GND	11
	GND	12

MAINBOARD CONNECT

P/N: 12G171000124

BLUETOOTH CABLE(WTB)

	GND	1	1
diff. 90ohm	BT_USBP	2	2
diff. 90ohm	BT_USBN	3	3
	NC	4	4
	BT_CHCLK	5	5
	BT_ON	6	6
	BT_DATA	7	7
	+3V_BT	8	8
	BT_LINK_LED	9	9
	GND	10	10

MAINBOARD CONNECT BlueTooth

P/N: 12G171000103

ASUS	Title : EMPTY	
ASUSTeK COMPUTER INC	Engineer: ENGINEER	
Size: Custom	Project Name: N10	Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 66 of 97	

LAUNCH CABLE(WTB)

+5V	14	14	+5V
+3VA	13	13	+3VA
GND	12	12	GND
LID_SW#	11	11	LID_SW#
PWRLED#	10	10	PWRLED#
PWR_SW#	9	9	PWR_SW#
GND	8	8	GND
MARATHON_SW#	7	7	MARATHON_SW#
MAGNIFY_SW#	6	6	MAGNIFY_SW#
+3VS	5	5	+3VS
HDLED#	4	4	HDLED#
NUM_LED#	3	3	NUM_LED#
CAP_LED#	2	2	CAP_LED#
+5VS	1	1	+5VS

MAINBOARD CONNECT **LAUNCH BOARD CONNECT**

P/N: 12G171000145 **P/N: 12G171030140**

MODEM CABLE(WTB)

RING	1		RING
TIP	2		TIP

MAINBOARD CONNECT **MODEM CONNECT**

FINGER-PRINTER CABLE(FFC)

GND	12	12	GND
FP_USB+	11	11	FP_USB+
FP_USB-	10	10	FP_USB-
+3VS	9	9	+3VS
NC	8	8	NC
NC	7	7	NC
GND	6	6	GND
GND	5	5	GND
TP_CLK	4	4	TP_CLK
TP_DAT	3	3	TP_DAT
+5VS_TP	2	2	+5VS_TP
+5VS_TP	1	1	+5VS_TP

MAINBOARD CONNECT **FINGER-PRINTER BOARD CONNECT**

P/N: 12G18340120C **P/N: 12G18340120C**

下接觸 下接觸

Touch-Pad CABLE(FFC)

+5VS	12	12	+5VS
+5VS	11	11	+5VS
TP_DAT	10	10	TP_DAT
TP_CLK	9	9	TP_CLK
GND	8	8	GND
GND	7	7	GND
NC	6	6	NC
NC	5	5	NC
NC	4	4	NC
SWL	3	3	SWL
SWR	2	2	SWR
NC	1	1	NC

FINGER-PRINTER BOARD CONNECT **Touch-Pad BOARD CONNECT**

P/N: 12G183301208

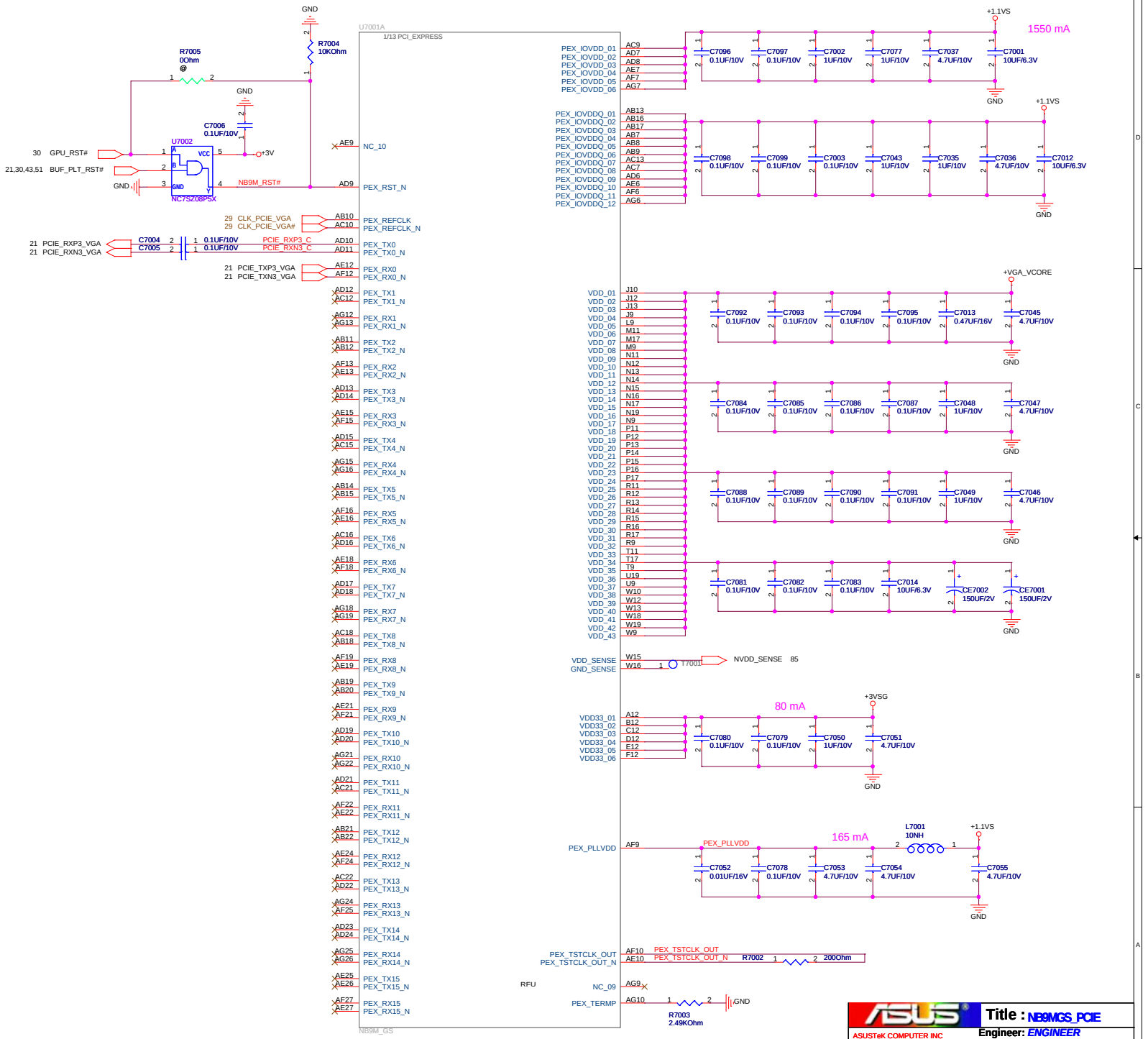
上接觸 上接觸

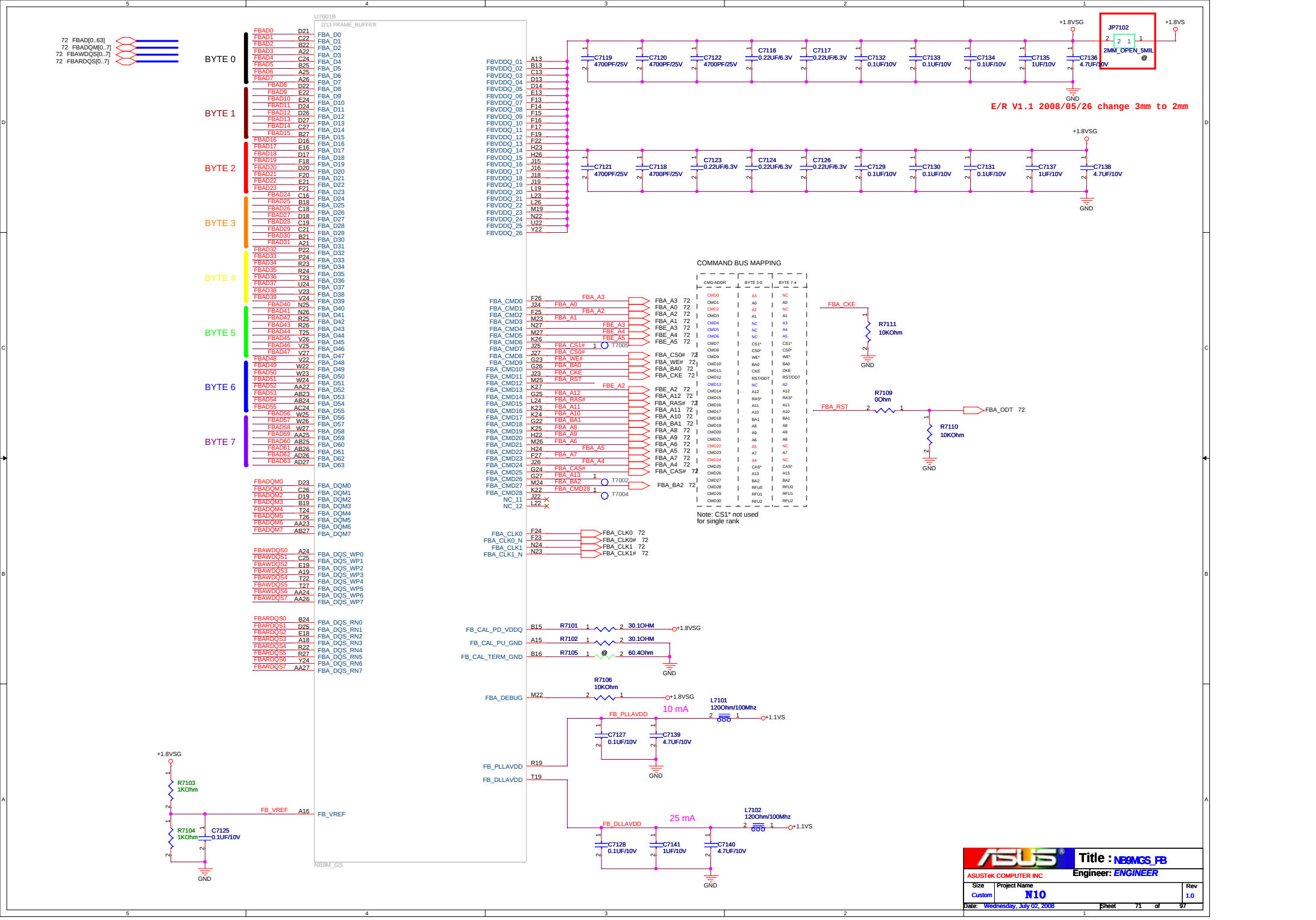
ASUS	Title : EMPTY	
ASUSTeK COMPUTER INC	Engineer: ENGINEER	
Size: Custom	Project Name: N10	Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 67 of 97	

ASUSTeK COMPUTER INC	Title : EMPTY	
	Engineer: ENGINEER	
Size: Custom	Project Name: N10	Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 68 of 97	

1.0 SR(2006/11/29)

ASUSTeK COMPUTER INC	Title : HISTORY		
	Engineer: ENGINEER		
Size: A	Project Name: N10		Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 69 of 97		


U7001A
1/13 PCI_EXPRESS
NB9M_GS
R7005
0Ohm
@
R7004
10KOhm
GND
C7006
0.1UF/10V
U7002
NC7SZ08P5X
30 GPU_RST#
21,30,43,51 BUF_PLT_RST#
+3V
NB9M_RST#
NC_10
PEX_RST_N
29 CLK_PCIE_VGA
29 CLK_PCIE_VGA#
PEX_REFCLK
PEX_REFCLK_N
21 PCIE_RXP3_VGA
21 PCIE_RXN3_VGA
C7004
C7005
0.1UF/10V
PCIE_RXP3_C
PCIE_RXN3_C
PEX_TX0
PEX_TX0_N
21 PCIE_TXP3_VGA
21 PCIE_TXN3_VGA
PEX_RX0
PEX_RX0_N
PEX_TX1
PEX_TX1_N
PEX_RX1
PEX_RX1_N
PEX_TX2
PEX_TX2_N
PEX_RX2
PEX_RX2_N
PEX_TX3
PEX_TX3_N
PEX_RX3
PEX_RX3_N
PEX_TX4
PEX_TX4_N
PEX_RX4
PEX_RX4_N
PEX_TX5
PEX_TX5_N
PEX_RX5
PEX_RX5_N
PEX_TX6
PEX_TX6_N
PEX_RX6
PEX_RX6_N
PEX_TX7
PEX_TX7_N
PEX_RX7
PEX_RX7_N
PEX_TX8
PEX_TX8_N
PEX_RX8
PEX_RX8_N
PEX_TX9
PEX_TX9_N
PEX_RX9
PEX_RX9_N
PEX_TX10
PEX_TX10_N
PEX_RX10
PEX_RX10_N
PEX_TX11
PEX_TX11_N
PEX_RX11
PEX_RX11_N
PEX_TX12
PEX_TX12_N
PEX_RX12
PEX_RX12_N
PEX_TX13
PEX_TX13_N
PEX_RX13
PEX_RX13_N
PEX_TX14
PEX_TX14_N
PEX_RX14
PEX_RX14_N
PEX_TX15
PEX_TX15_N
PEX_RX15
PEX_RX15_N
PEX_IOVDD_01
PEX_IOVDD_02
PEX_IOVDD_03
PEX_IOVDD_04
PEX_IOVDD_05
PEX_IOVDD_06
+1.1VS
1550 mA
C7096 0.1UF/10V
C7097 0.1UF/10V
C7002 1UF/10V
C7077 1UF/10V
C7037 4.7UF/10V
C7001 10UF/6.3V
PEX_IOVDDQ_01
PEX_IOVDDQ_02
PEX_IOVDDQ_03
PEX_IOVDDQ_04
PEX_IOVDDQ_05
PEX_IOVDDQ_06
PEX_IOVDDQ_07
PEX_IOVDDQ_08
PEX_IOVDDQ_09
PEX_IOVDDQ_10
PEX_IOVDDQ_11
PEX_IOVDDQ_12
C7098 0.1UF/10V
C7099 0.1UF/10V
C7003 0.1UF/10V
C7043 1UF/10V
C7035 1UF/10V
C7036 4.7UF/10V
C7012 10UF/6.3V
+VGA_VCORE
VDD_01
VDD_02
VDD_03
VDD_04
VDD_05
VDD_06
VDD_07
VDD_08
VDD_09
VDD_10
VDD_11
VDD_12
VDD_13
VDD_14
VDD_15
VDD_16
VDD_17
VDD_18
VDD_19
VDD_20
VDD_21
VDD_22
VDD_23
VDD_24
VDD_25
VDD_26
VDD_27
VDD_28
VDD_29
VDD_30
VDD_31
VDD_32
VDD_33
VDD_34
VDD_35
VDD_36
VDD_37
VDD_38
VDD_39
VDD_40
VDD_41
VDD_42
VDD_43
C7092 0.1UF/10V
C7093 0.1UF/10V
C7094 0.1UF/10V
C7095 0.1UF/10V
C7013 0.47UF/16V
C7045 4.7UF/10V
C7084 0.1UF/10V
C7085 0.1UF/10V
C7086 0.1UF/10V
C7087 0.1UF/10V
C7048 1UF/10V
C7047 4.7UF/10V
C7088 0.1UF/10V
C7089 0.1UF/10V
C7090 0.1UF/10V
C7091 0.1UF/10V
C7049 1UF/10V
C7046 4.7UF/10V
C7081 0.1UF/10V
C7082 0.1UF/10V
C7083 0.1UF/10V
C7014 10UF/6.3V
CE7002 150UF/2V
CE7001 150UF/2V
VDD_SENSE
GND_SENSE
T7001
NVDD_SENSE 85
+3VSG
80 mA
VDD33_01
VDD33_02
VDD33_03
VDD33_04
VDD33_05
VDD33_06
C7080 0.1UF/10V
C7079 0.1UF/10V
C7050 1UF/10V
C7051 4.7UF/10V
PEX_PLLVDD
165 mA
L7001
10NH
C7052 0.01UF/16V
C7078 0.1UF/10V
C7053 4.7UF/10V
C7054 4.7UF/10V
C7055 4.7UF/10V
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT_N
R7002
200Ohm
RFU
NC_09
PEX_TERMP
R7003
2.49KOhm
Title : NB9MGS_PCIE
ASUSTeK COMPUTER INC
Engineer: ENGINEER
Size
Custom
Project Name
N10
Rev
1.0
Date: Wednesday, July 02, 2008
Sheet 70 of 97


U7001B
2/13 FRAME_BUFFER
72 FBAD[0..63]
72 FBADQM[0..7]
72 FBAWDQS[0..7]
72 FBARDQS[0..7]
BYTE 0
BYTE 1
BYTE 2
BYTE 3
BYTE 4
BYTE 5
BYTE 6
BYTE 7
+1.8VSG
JP7102
2MM_OPEN_5MIL
+1.8VS
C7119 4700PF/25V
C7120 4700PF/25V
C7122 4700PF/25V
C7116 0.22UF/6.3V
C7117 0.22UF/6.3V
C7132 0.1UF/10V
C7133 0.1UF/10V
C7134 0.1UF/10V
C7135 1UF/10V
C7136 4.7UF/10V
GND
E/R V1.1 2008/05/26 change 3mm to 2mm
C7121 4700PF/25V
C7118 4700PF/25V
C7123 0.22UF/6.3V
C7124 0.22UF/6.3V
C7126 0.22UF/6.3V
C7129 0.1UF/10V
C7130 0.1UF/10V
C7131 0.1UF/10V
C7137 1UF/10V
C7138 4.7UF/10V
COMMAND BUS MAPPING
CMD-ADDR
BYTE 3-0
BYTE 7-4
Note: CS1* not used for single rank
FBA_CKE
R7111 10KOhm
R7109 0Ohm
FBA_RST
FBA_ODT 72
R7110 10KOhm
FBA_CLK0
FBA_CLK0_N
FBA_CLK1
FBA_CLK1_N
FBA_CLK0 72
FBA_CLK0# 72
FBA_CLK1 72
FBA_CLK1# 72
FBADQM0
FBADQM1
FBADQM2
FBADQM3
FBADQM4
FBADQM5
FBADQM6
FBADQM7
FBA_DQM0
FBA_DQM1
FBA_DQM2
FBA_DQM3
FBA_DQM4
FBA_DQM5
FBA_DQM6
FBA_DQM7
FBAWDQS0
FBAWDQS1
FBAWDQS2
FBAWDQS3
FBAWDQS4
FBAWDQS5
FBAWDQS6
FBAWDQS7
FBA_DQS_WP0
FBA_DQS_WP1
FBA_DQS_WP2
FBA_DQS_WP3
FBA_DQS_WP4
FBA_DQS_WP5
FBA_DQS_WP6
FBA_DQS_WP7
FBARDQS0
FBARDQS1
FBARDQS2
FBARDQS3
FBARDQS4
FBARDQS5
FBARDQS6
FBARDQS7
FBA_DQS_RN0
FBA_DQS_RN1
FBA_DQS_RN2
FBA_DQS_RN3
FBA_DQS_RN4
FBA_DQS_RN5
FBA_DQS_RN6
FBA_DQS_RN7
FB_CAL_PD_VDDQ
FB_CAL_PU_GND
FB_CAL_TERM_GND
R7101 30.1OHM
R7102 30.1OHM
R7105 60.4Ohm
FBA_DEBUG
R7106 10KOhm
L7101 120Ohm/100Mhz
10 mA
FB_PLLAVDD
C7127 0.1UF/10V
C7139 4.7UF/10V
FB_DLLAVDD
L7102 120Ohm/100Mhz
25 mA
C7128 0.1UF/10V
C7141 1UF/10V
C7140 4.7UF/10V
+1.1VS
R7103 1KOhm
R7104 1KOhm
C7125 0.1UF/10V
FB_VREF
NB9M_GS
ASUSTeK COMPUTER INC
Title : NB9MGS_FB
Engineer: ENGINEER
Size Custom
Project Name N10
Rev 1.0
Date: Wednesday, July 02, 2008
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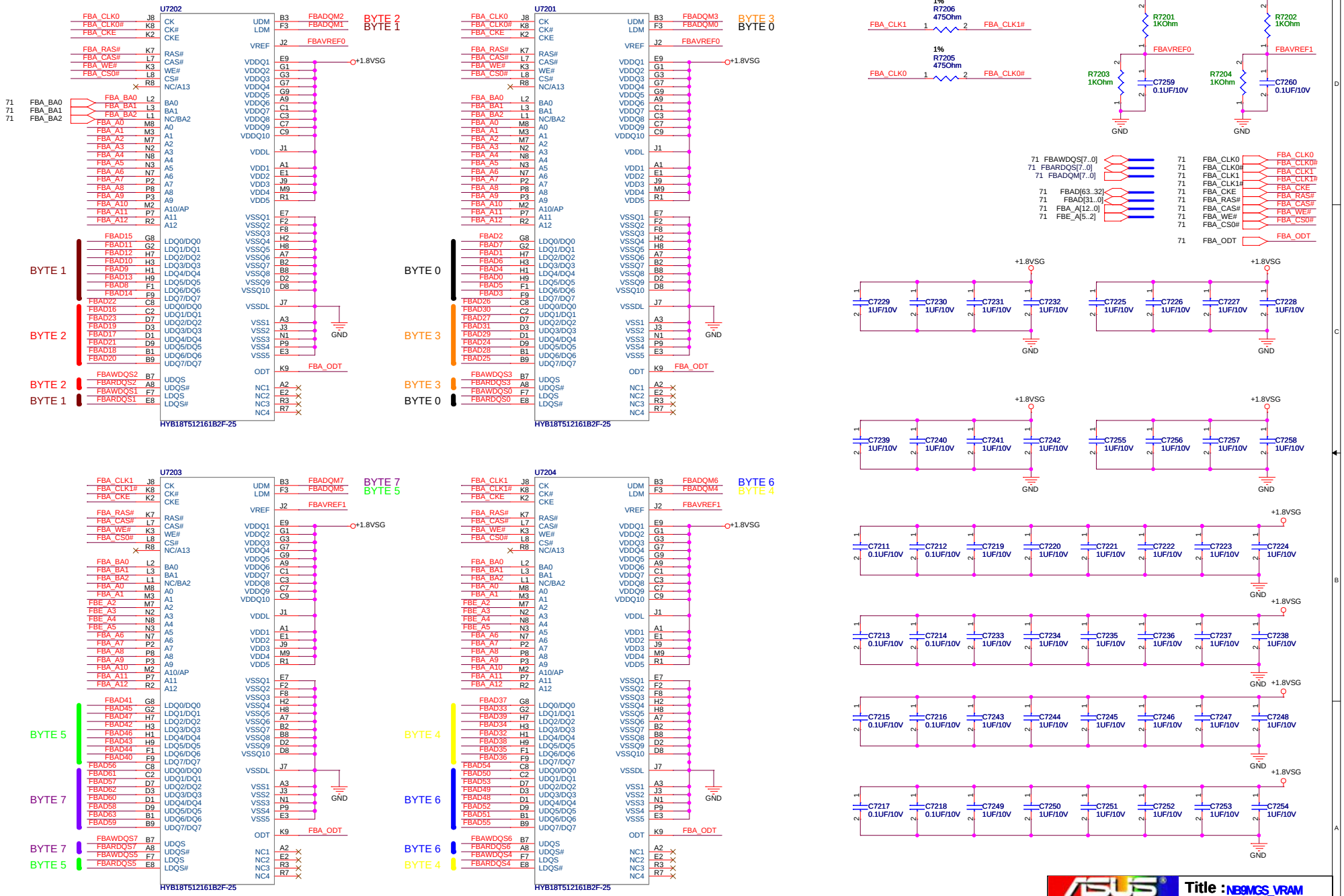
U7202
U7201
U7203
U7204
HYB18T512161B2F-25
BYTE 2
BYTE 1
BYTE 0
BYTE 3
BYTE 7
BYTE 5
BYTE 6
BYTE 4
+1.8VSG
GND
FBA_ODT
FBAVREF0
FBAVREF1
FBADQM2
FBADQM1
FBADQM3
FBADQM0
FBADQM7
FBADQM5
FBADQM6
FBADQM4
FBA_CLK1
FBA_CLK1#
FBA_CLK0
FBA_CLK0#
1%
R7206
475Ohm
R7205
475Ohm
R7201
1KOhm
R7202
1KOhm
R7203
1KOhm
R7204
1KOhm
C7259
0.1UF/10V
C7260
0.1UF/10V
FBAWDQS[7..0]
FBARDQS[7..0]
FBADQM[7..0]
FBAD[63..32]
FBAD[31..0]
FBA_A[12..0]
FBE_A[5..2]
FBA_CLK0
FBA_CLK0#
FBA_CLK1
FBA_CLK1#
FBA_CKE
FBA_RAS#
FBA_CAS#
FBA_WE#
FBA_CS0#
FBA_ODT
C7229 1UF/10V
C7230 1UF/10V
C7231 1UF/10V
C7232 1UF/10V
C7225 1UF/10V
C7226 1UF/10V
C7227 1UF/10V
C7228 1UF/10V
C7239 1UF/10V
C7240 1UF/10V
C7241 1UF/10V
C7242 1UF/10V
C7255 1UF/10V
C7256 1UF/10V
C7257 1UF/10V
C7258 1UF/10V
C7211 0.1UF/10V
C7212 0.1UF/10V
C7219 1UF/10V
C7220 1UF/10V
C7221 1UF/10V
C7222 1UF/10V
C7223 1UF/10V
C7224 1UF/10V
C7213 0.1UF/10V
C7214 0.1UF/10V
C7233 1UF/10V
C7234 1UF/10V
C7235 1UF/10V
C7236 1UF/10V
C7237 1UF/10V
C7238 1UF/10V
C7215 0.1UF/10V
C7216 0.1UF/10V
C7243 1UF/10V
C7244 1UF/10V
C7245 1UF/10V
C7246 1UF/10V
C7247 1UF/10V
C7248 1UF/10V
C7217 0.1UF/10V
C7218 0.1UF/10V
C7249 1UF/10V
C7250 1UF/10V
C7251 1UF/10V
C7252 1UF/10V
C7253 1UF/10V
C7254 1UF/10V
Title : NB9MGS_VRAM
ASUSTeK COMPUTER INC
Engineer: ENGINEER
Size
Custom
Project Name
N10
Rev
1.0
Date: Wednesday, July 02, 2008
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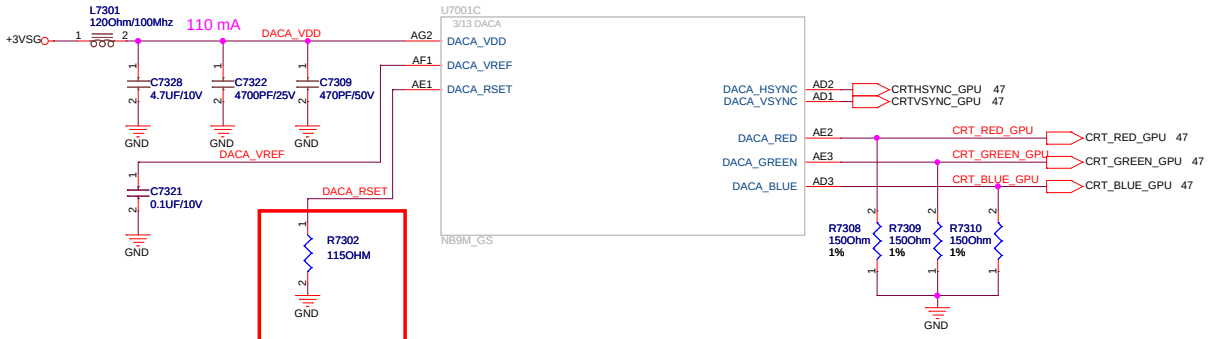
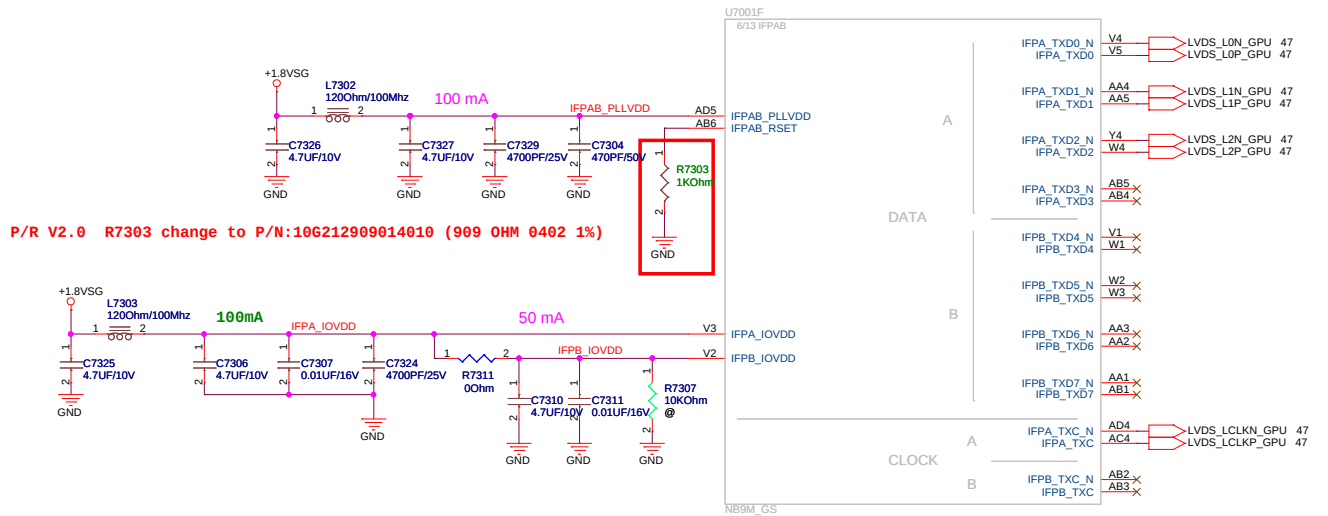
VGA

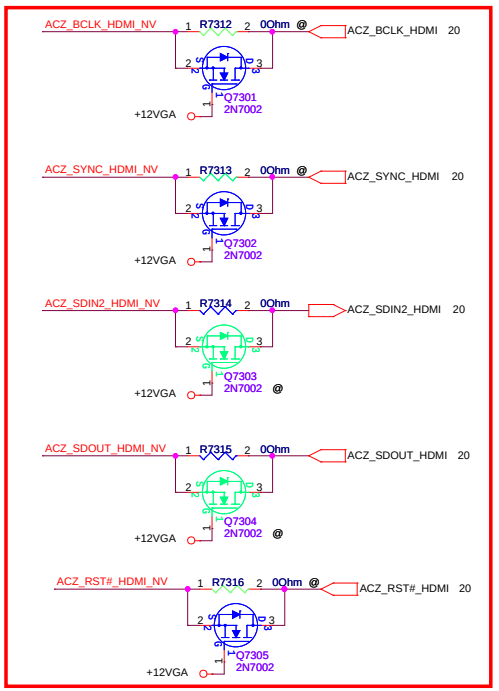


P/R V2.0 2008/6/30 R7302 change P/N

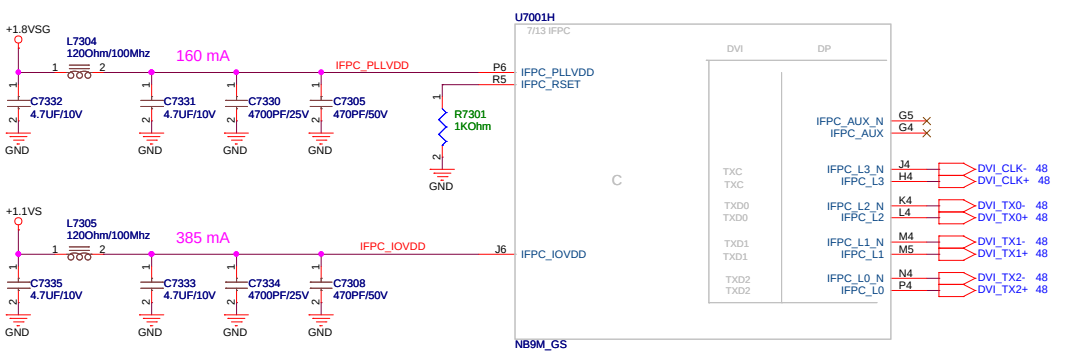
LVDS

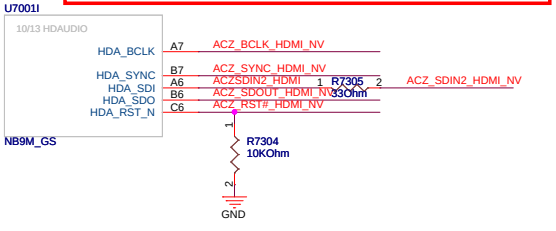


P/R V2.0 R7303 change to P/N:10G212909014010 (909 OHM 0402 1%)



HDMI

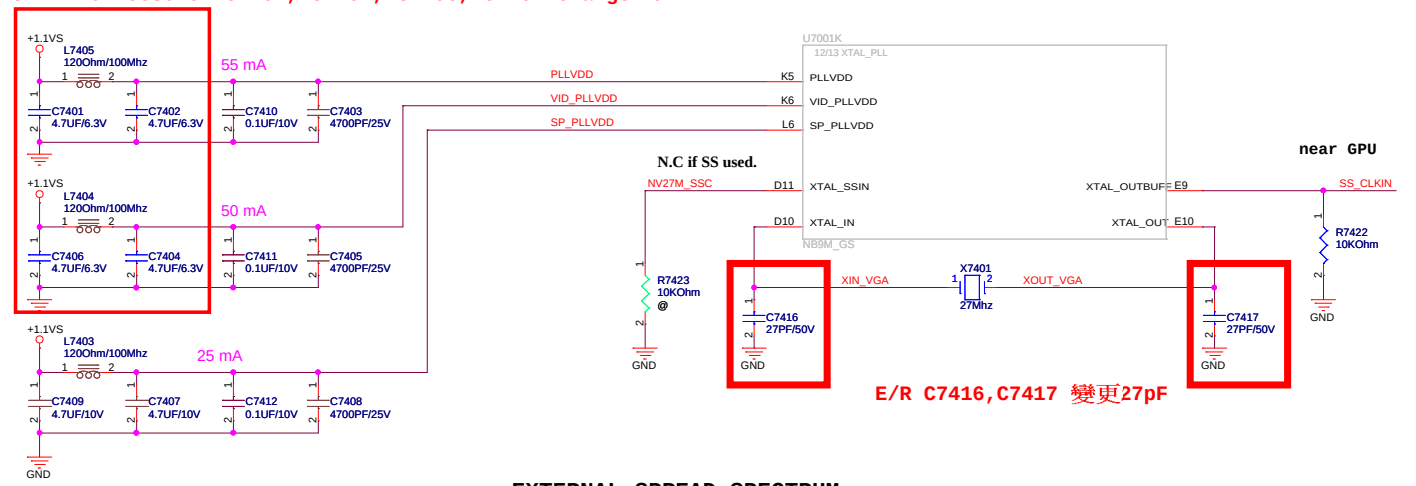




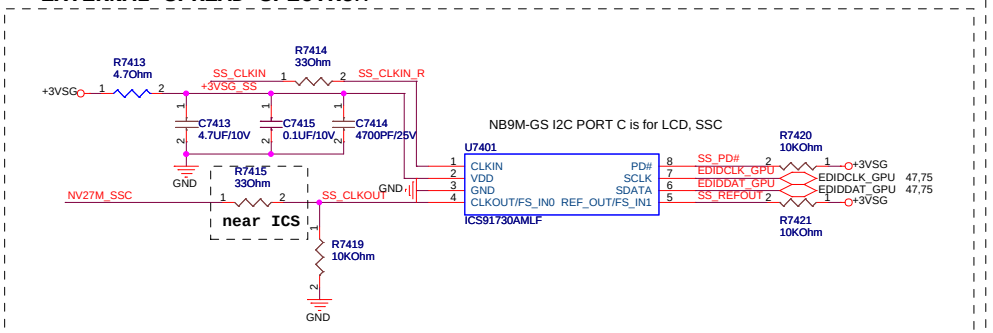
ASUSTeK COMPUTER INC	Title : NB9MGS_DISPLAY	
	Engineer: ENGINEER	
Size: Custom	Project Name: N10	Rev: 1.0
Date: Monday, July 07, 2008	Sheet 73 of 97	

Xtal

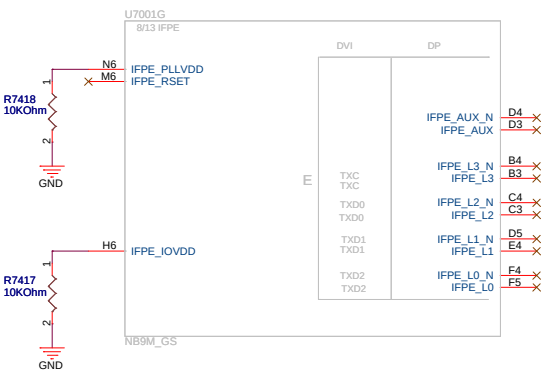
P/R V2.0 20080701 C7401, C7402, C7406, C7404 change P/N

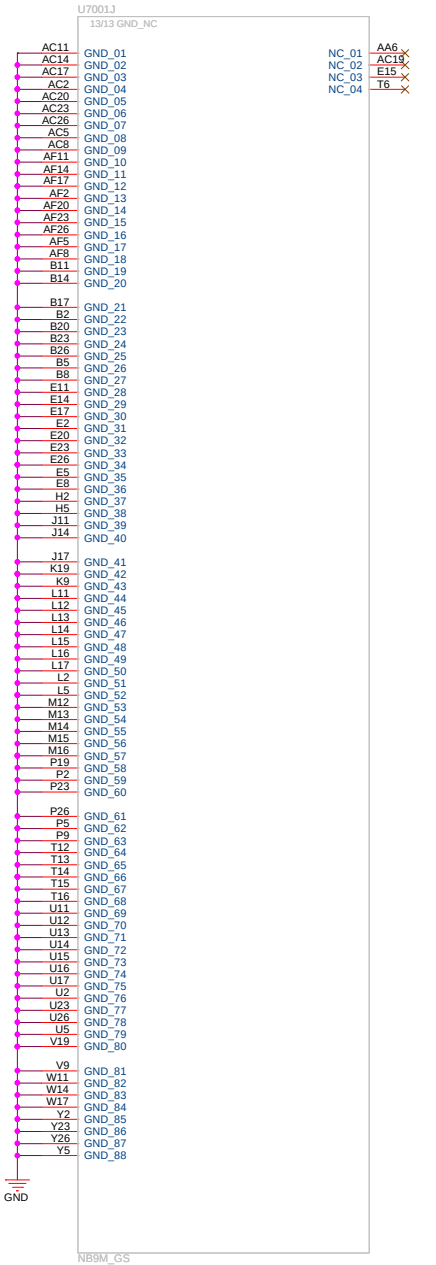


EXTERNAL SPREAD SPECTRUM



Other

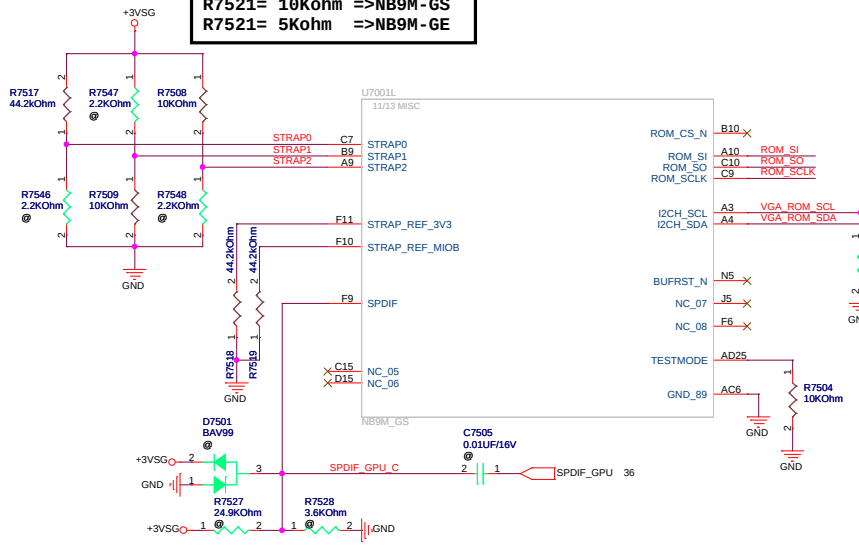


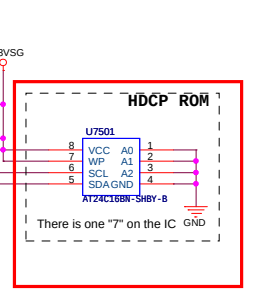


ASUSTeK COMPUTER INC	Title : NB9MGS_XTAL	Engineer: ENGINEER
Size: Custom	Project Name: N10	Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 74 of 97	

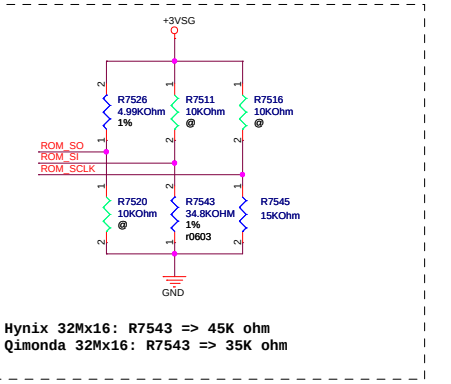
ROM

R7521= 10Kohm =>NB9M-GS
R7521= 5Kohm =>NB9M-GE





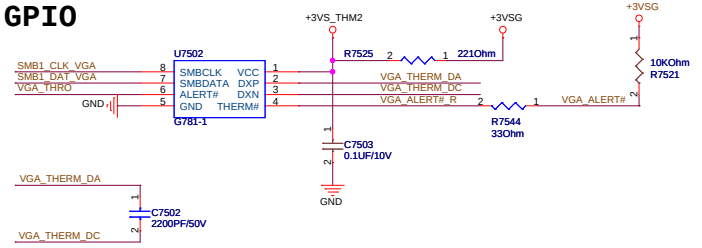
E/R V1.1 2008/5/28 U7501 change P/N: 05G021402019

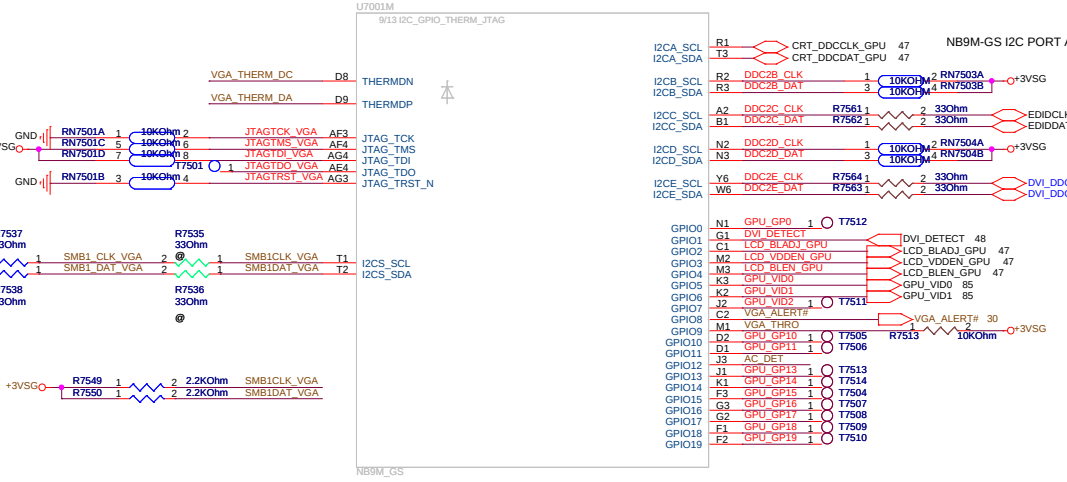


Hynix 32Mx16: R7543 => 45K ohm
Qimonda 32Mx16: R7543 => 35K ohm

External thermal sensor

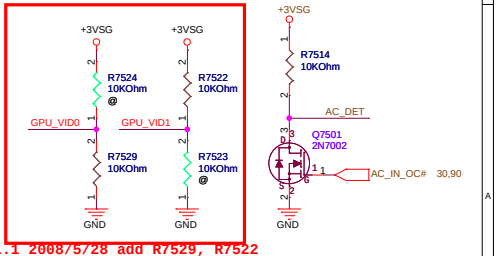
GPIO





GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	N/A
1	IN	N/A	HDMI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID 0
6	OUT	N/A	NVVDD VID 1
7	OUT	N/A	FBVDD VID 0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	Low	SLI SYNCO
12	IN	N/A	AC DETECT
13	OUT	N/A	PS CONTROL
14	OUT	N/A	PS CONTROL



E/R V1.1 2008/5/28 add R7529, R7522

ASUSTeK COMPUTER INC

Title : NB9MGS_ROM

Engineer: ENGINEER

Size	Project Name	Rev
Custom	N10	1.0

Date: Wednesday, July 02, 2008 Sheet 75 of 97

ASUSTeK COMPUTER INC	Title : EMPTY		
	Engineer: ENGINEER		
Size: A	Project Name: N10		Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 76 of 97		

ASUSTeK COMPUTER INC	Title : ****	
	Engineer: ENGINEER	
Size: Custom	Project Name: N10	Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 77 of 97	

ASUSTeK COMPUTER INC	Title : ****
	Engineer: *ENGINEER*
Size: B	Project Name: **N10 FUNC BOARD**
	Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 78 of 97

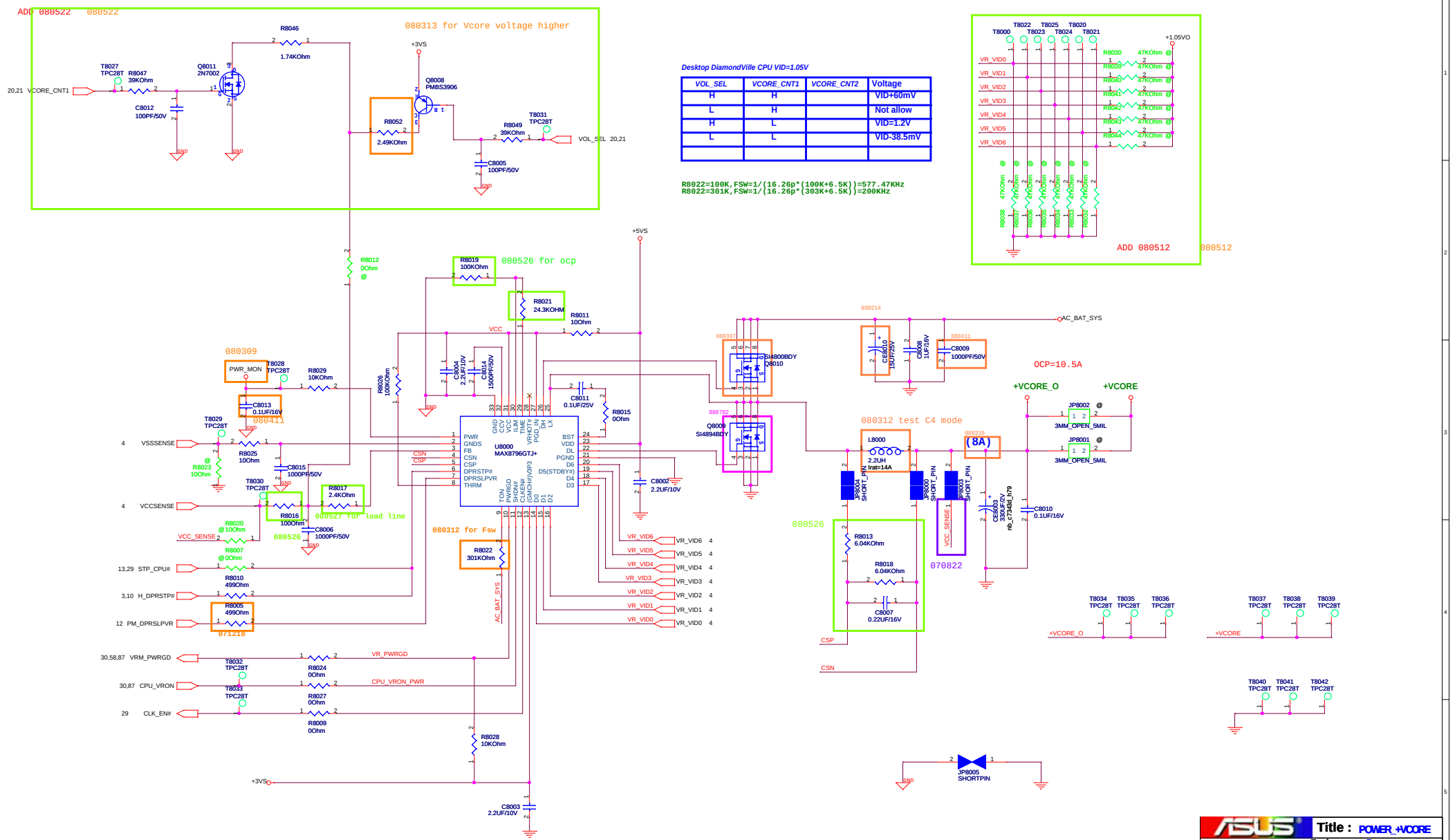
Title : ****

ASUSTeK COMPUTER INC

Engineer: ENGINEER

Size	Project Name	Rev
B	N10 POWER SW	1.0

Date: Wednesday, July 02, 2008



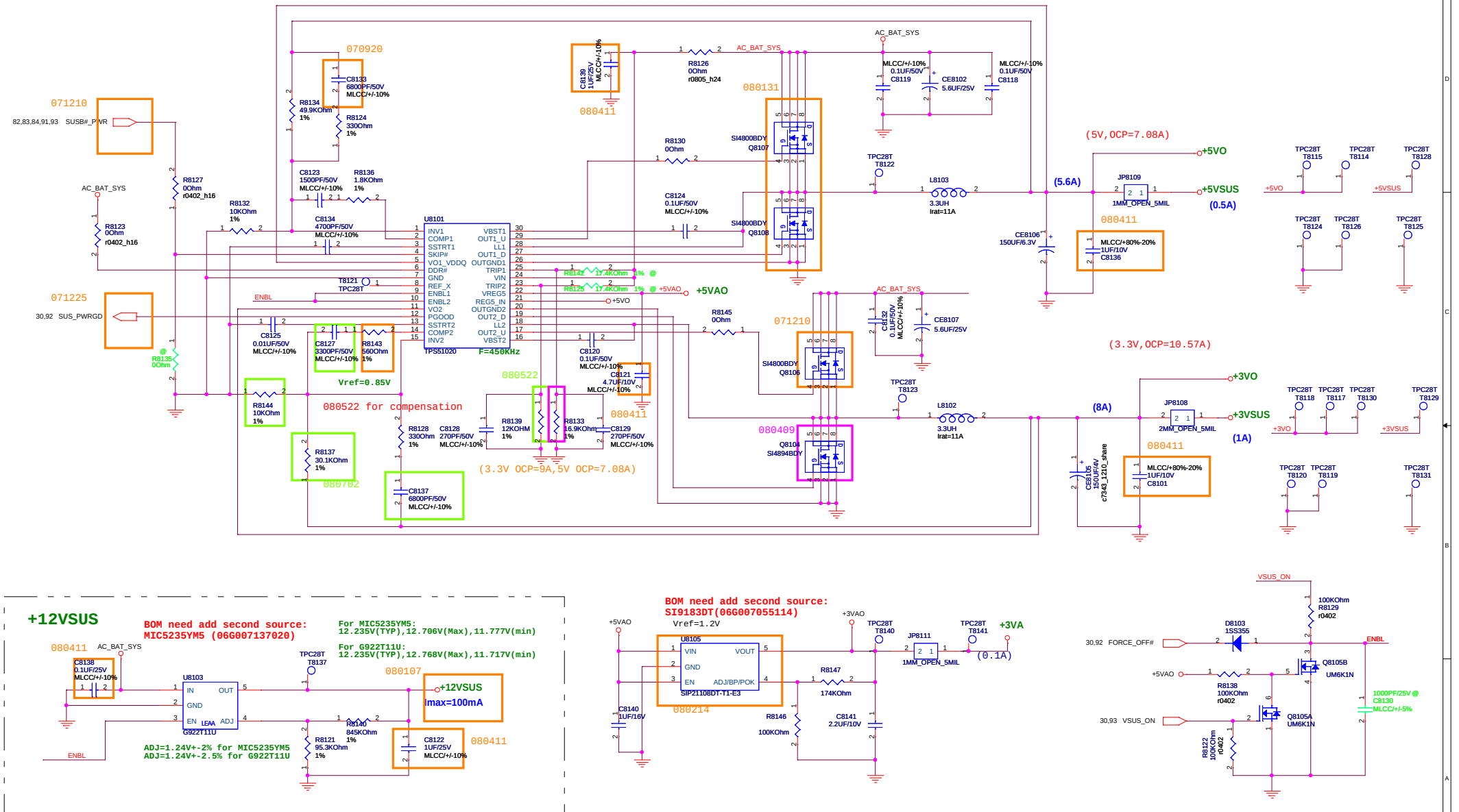
ASUSTek COMPUTER INC. NB6

Title : POWER +VCORE

Engineer: Benson

Size	Project Name	Rev
Custom	N10	1.0

Date: Wednesday, July 02, 2008 Sheet 80 of 97



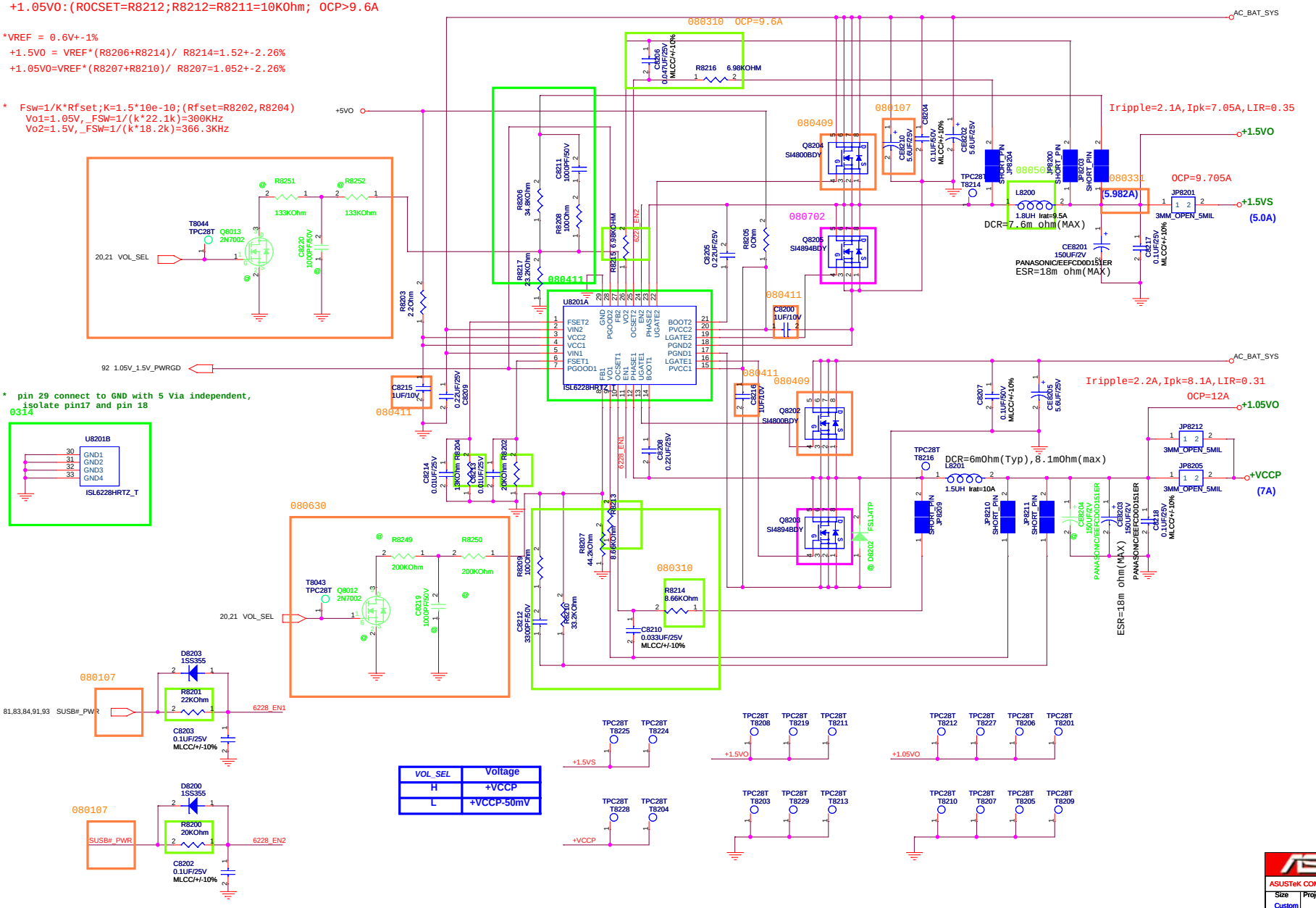
Title : POWER_SYSTEM		
ASUSTek COMPUTER INC. NB6	Engineer: Benson	
Size: Custom	Project Name: N10	Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 81 of 97	

VOL_SEL	Voltage
H	+1.5VS
L	+1.5VS-75mV

*Rocset=Ioc*DCR/10uA,(ROCSET=R8213;R8215=R8213)
+1.5VO:(ROCSET=R8213;R8215=R8213=10.7KOhm; OCP>6A
+1.05VO:(ROCSET=R8212;R8212=R8211=10KOhm; OCP>9.6A

*VREF = 0.6V+-1%
+1.5VO = VREF*(R8206+R8214)/ R8214=1.52+-2.26%
+1.05VO=VREF*(R8207+R8210)/ R8207=1.052+-2.26%

* Fsw=1/K*Rfset;K=1.5*10e-10;(Rfset=R8202,R8204)
Vo1=1.05V, _FSW=1/(k*22.1k)=300KHz
Vo2=1.5V, _FSW=1/(k*18.2k)=366.3KHz



VOL_SEL	Voltage
H	+VCCP
L	+VCCP-50mV

ASUSTeK COMPUTER INC

Title : POWER_IO_VCCP&1.5VS

Engineer: Benson

Size	Project Name	Rev
Custom	N10	1.0

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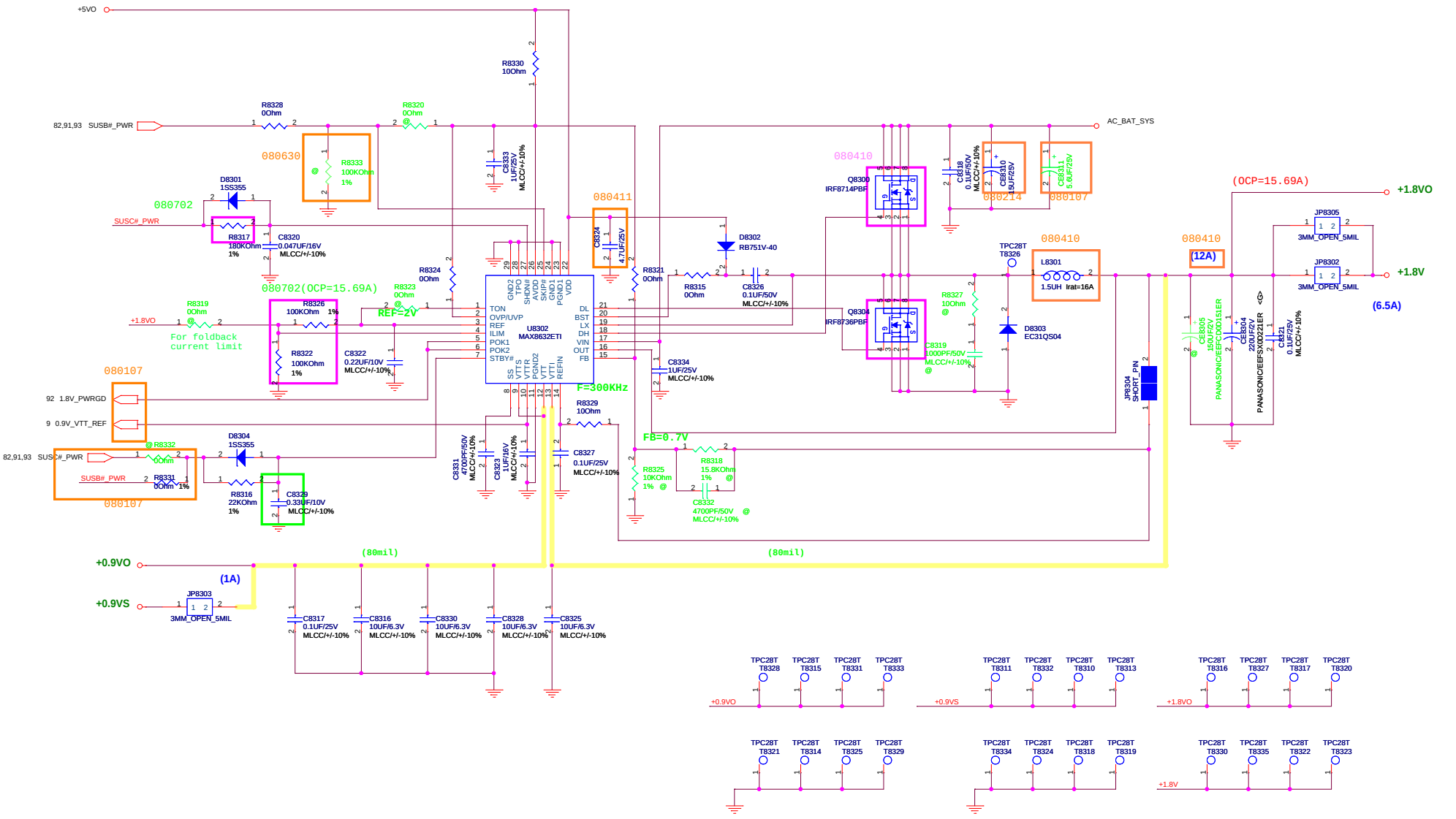
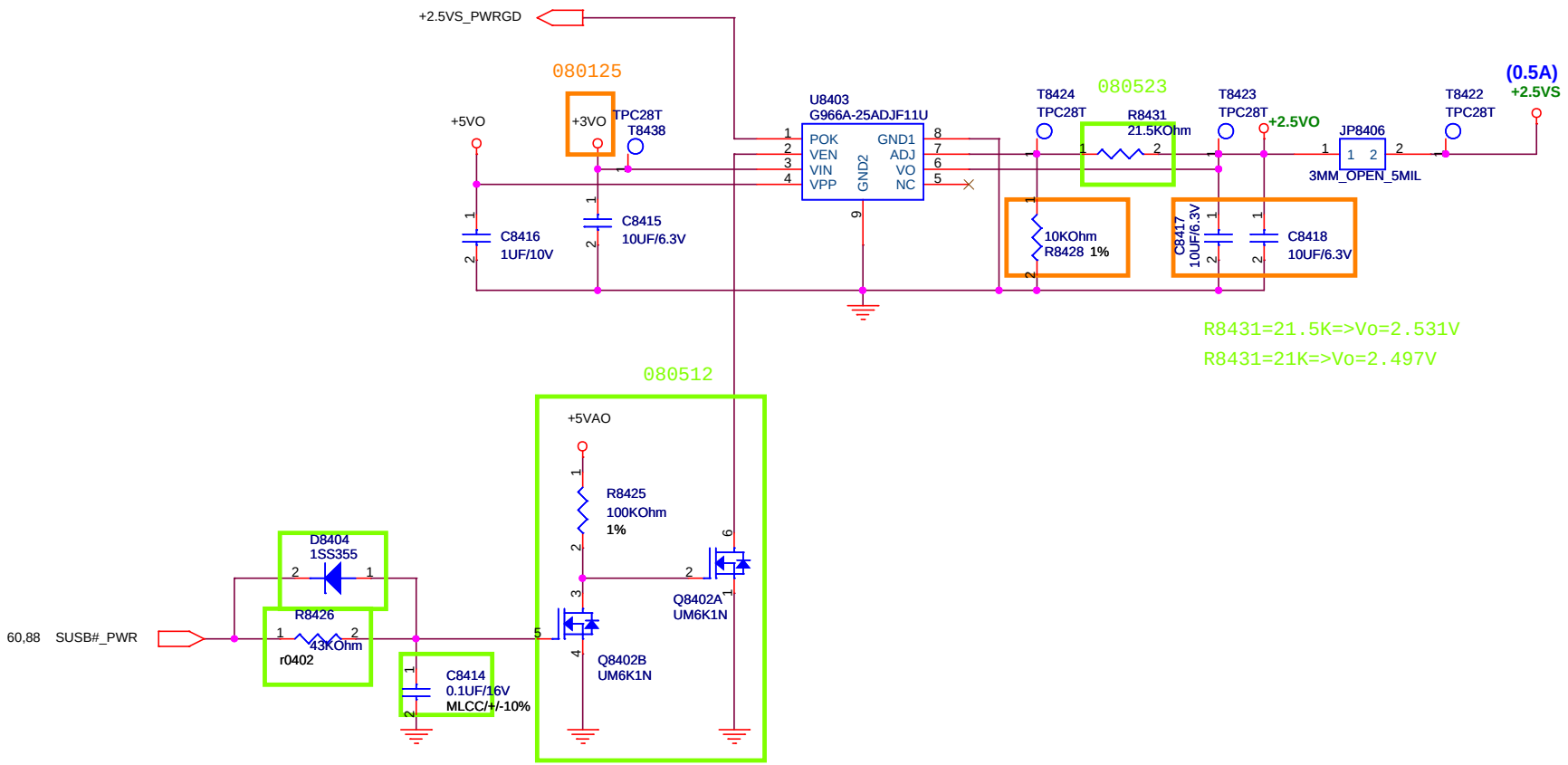
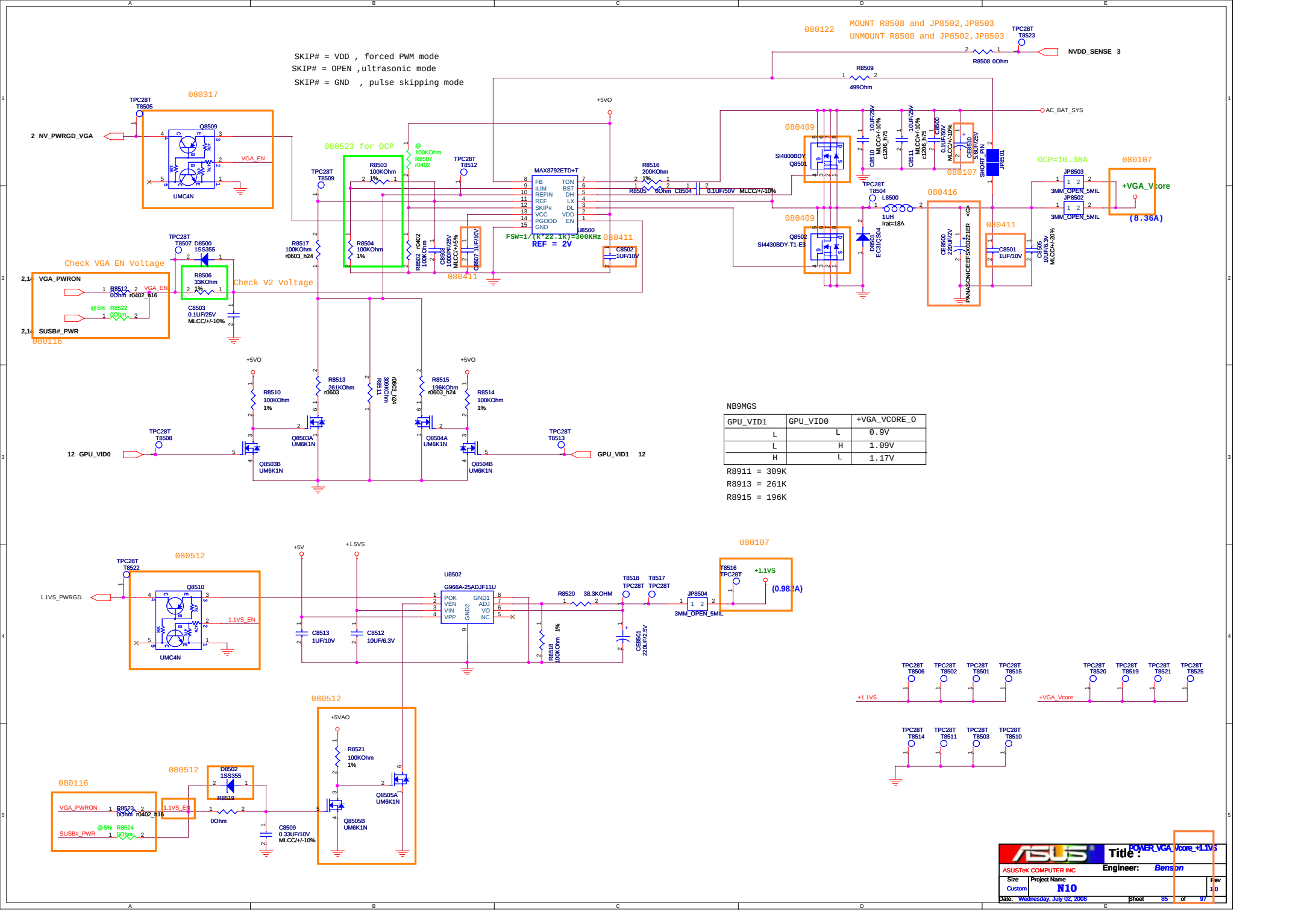


ASUSTeK COMPUTER INC	Title : POWER_I/O_1.8V & 0.9VS		
	Engineer: Benson		
Size: Custom	Project Name: N10		Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 83 of 97		

+2.5VS



ASUS	Title : POWER_2.5VS&3VA	
ASUSTeK COMPUTER INC	Engineer: Benson	
Size: Custom	Project Name: N10	Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 84 of 97	


SKIP# = VDD , forced PWM mode
SKIP# = OPEN ,ultrasonic mode
SKIP# = GND , pulse skipping mode
080122
MOUNT R8508 and JP8502,JP8503
UNMOUNT R8508 and JP8502,JP8503
TPC28T T8523
NVDD_SENSE 3
R8508 0Ohm
R8509 499Ohm
AC_BAT_SYS
080317
TPC28T T8505
2 NV_PWRGD_VGA
Q8509
VGA_EN
UMC4N
080523 for OCP
R8503 100KOhm 1%
@ 100KOhm R8507 r0402
TPC28T T8512
TPC28T T8509
MAX8792ETD+T
FB TON ILIM BST REFIN DH REF LX SKIP# DL VCC VDD PGOOD EN GND
U8500
FSW=1/(K*22.1k)=300KHz
REF = 2V
R8516 200KOhm 1%
R8505 0Ohm C8504 0.1UF/50V MLCC/+/-10%
+5VO
080409
SI4800BDY Q8501
SI4430BDY-T1-E3
080411
C8502 1UF/10V
C8507 1UF/10V
C8508 1000PF/25V MLCC/+/-5%
R8502 r0402 100KOhm
R8504 100KOhm 1%
R8517 100KOhm r0603_h24
TPC28T T8507 D8500 1SS355
Check VGA EN Voltage
Check V2 Voltage
VGA_PWRON
SUSB#_PWR
R8512 0Ohm r0402_h16
@5% R8522 0Ohm
R8506 33KOhm 1%
C8503 0.1UF/25V MLCC/+/-10%
080116
TPC28T T8504
L8500 1UH Irat=18A
D8501 EC33Q304
080416
CE8500 220UF/2V
PANASONICEEFSX0D221ER
080411
C8501 1UF/10V
CE8505 10UF/6.3V MLCC/+/-20%
C8510 10UF/25V MLCC/+/-10% c1206_h75
C8511 10UF/25V MLCC/+/-10% c1206_h75
CE8500 0.1UF/50V MLCC/+/-10%
CE8510 5.6UF/25V
JP8501 SHORT_PIN
OCP=10.38A
080107
JP8503 3MM_OPEN_5MIL
JP8502 3MM_OPEN_5MIL
+VGA_Vcore
(8.36A)
R8510 100KOhm 1%
R8513 261KOhm r0603
R8511 309KOhm r0603_h24
R8515 196KOhm r0603_h24
R8514 100KOhm 1%
Q8503A UM6K1N
Q8504A UM6K1N
Q8503B UM6K1N
Q8504B UM6K1N
TPC28T T8508
12 GPU_VID0
TPC28T T8513
GPU_VID1 12
NB9MGS
R8911 = 309K
R8913 = 261K
R8915 = 196K
080512
TPC28T T8522
1.1VS_PWRGD
Q8510
1.1VS_EN
UMC4N
+5V
+1.5VS
C8513 1UF/10V
C8512 10UF/6.3V
U8502
G966A-25ADJF11U
POK GND1 VEN ADJ VIN VO VPP GND2 NC
R8520 38.3KOHM
T8518 TPC28T
T8517 TPC28T
JP8504 3MM_OPEN_5MIL
T8516 TPC28T
+1.1VS
(0.98A)
R8518 100KOhm 1%
CE8501 220UF/2.5V
+5VAO
R8521 100KOhm 1%
Q8505A UM6K1N
Q8505B UM6K1N
D8502 1SS355
R8519 0Ohm
C8509 0.33UF/10V MLCC/+/-10%
VGA_PWRON
SUSB#_PWR
R8523 0Ohm r0402_h16
@5% R8524 0Ohm
TPC28T T8506 TPC28T T8502 TPC28T T8501 TPC28T T8515
+1.1VS
TPC28T T8520 TPC28T T8519 TPC28T T8521 TPC28T T8525
+VGA_Vcore
TPC28T T8514 TPC28T T8511 TPC28T T8503 TPC28T T8510
ASUSTeK COMPUTER INC
Title : POWER_VGA_Vcore_+1.1VS
Engineer: Benson
Size Custom
Project Name N10
Rev 1.0
Date: Wednesday, July 02, 2008
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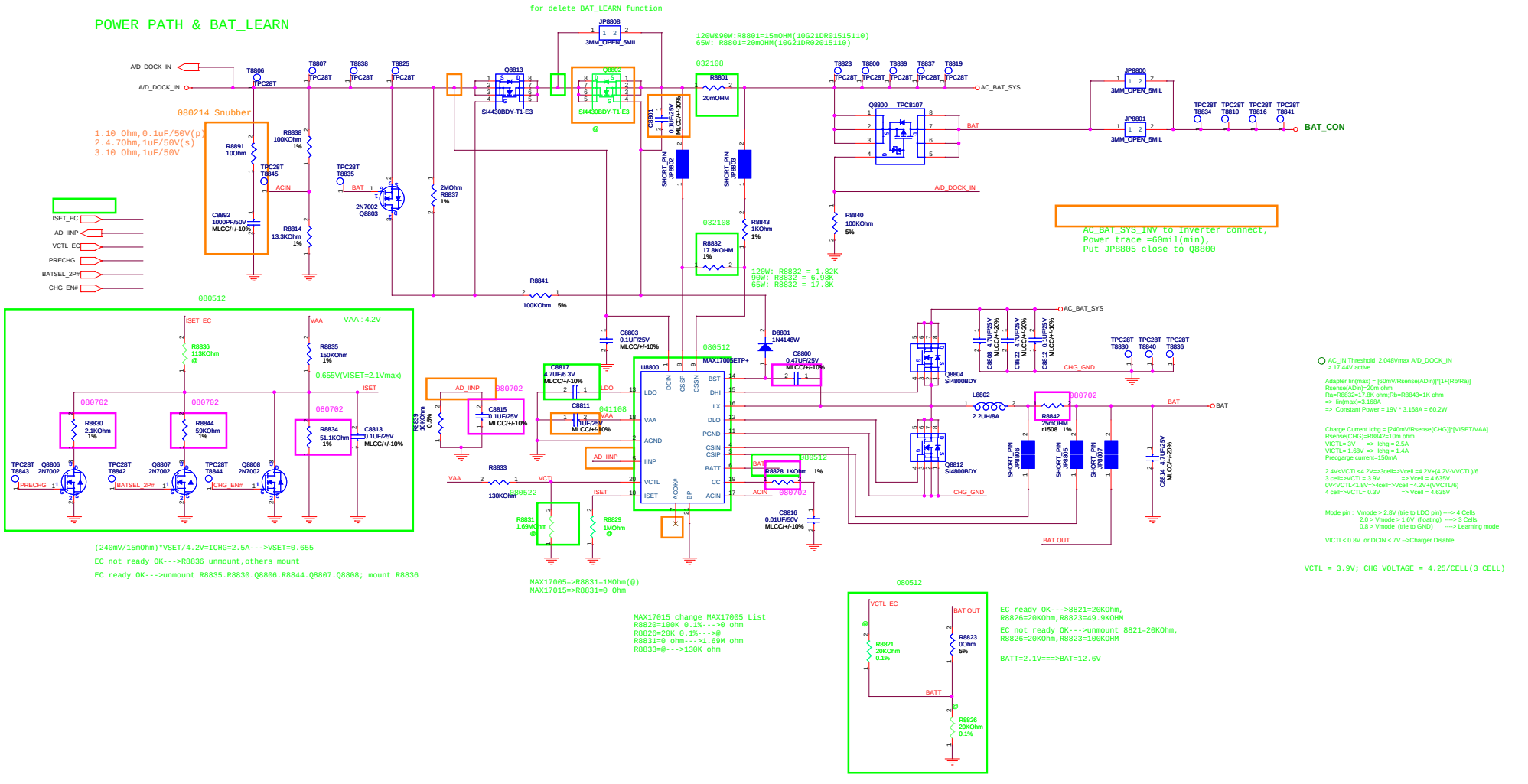
ASUSTeK COMPUTER INC	Title : N/A		
	Engineer: Benson		
Size A	Project Name N10		Rev 1.0
Date: Wednesday, July 02, 2008		Sheet 86 of 97	

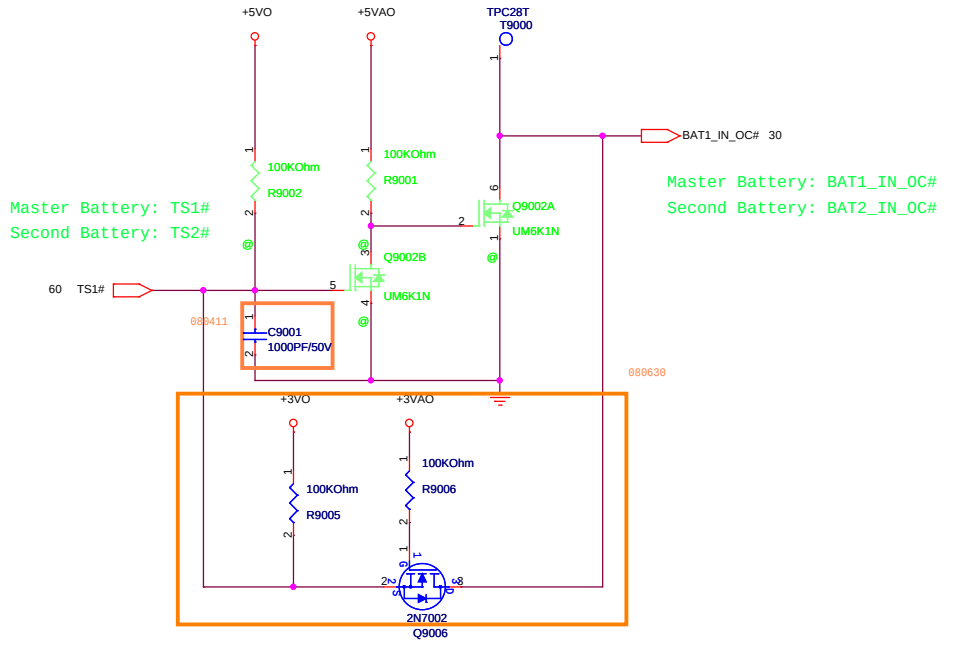
ASUSTeK COMPUTER INC	Title : POWER_SHUTDOWN#		
	Engineer: Benson		
Size: A	Project Name: N10		Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 87 of 97		



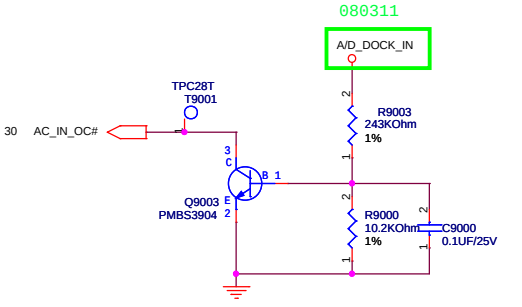
ASUS	Title : POWER_CHARGER		
<OrgName>	Engineer: Benson		
Size: Custom	Project Name: N10		Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 88 of 97		

Title : N/A			
ASUSTeK COMPUTER INC	Engineer: Benson		
Size A	Project Name N10		Rev 1.0
Date: Wednesday, July 02, 2008	Sheet 89 of 97		

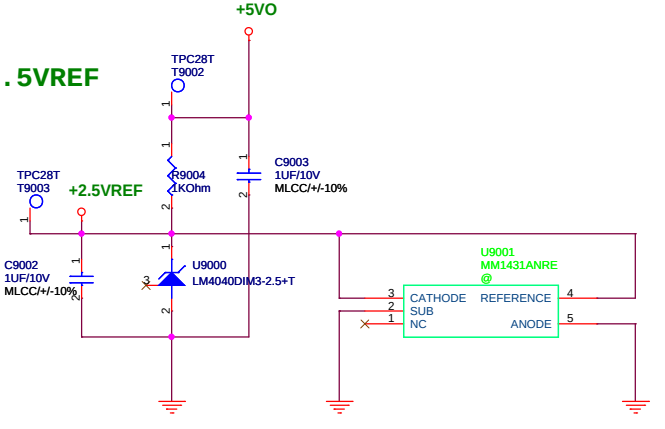
BATTERY IN DETECT



ADAPTER IN DETECT



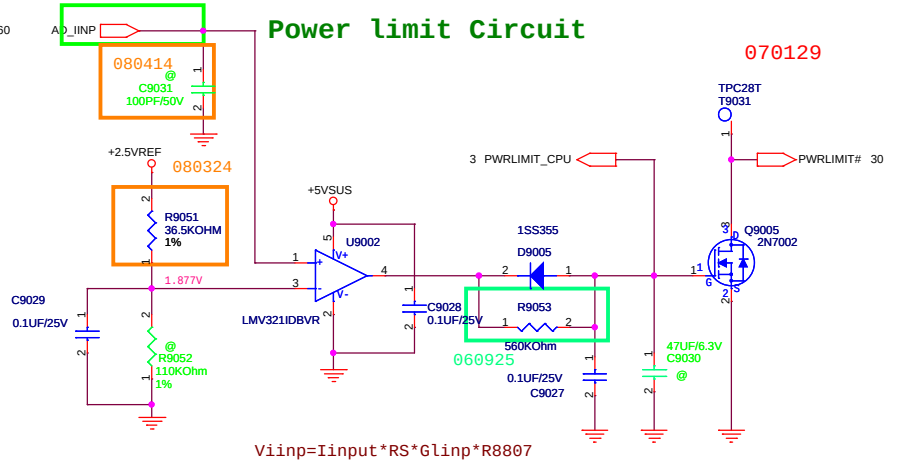
+2.5VREF



U8600 & U8601 colay

U8600 Main source change to 06G006002414(tolerence:1%).
Add second source 06G006002610 (tolerence:1%),
06G006002412 (tolerence:0.2%) and
06G006002020(tolerence:0.2%)

Power limit Circuit

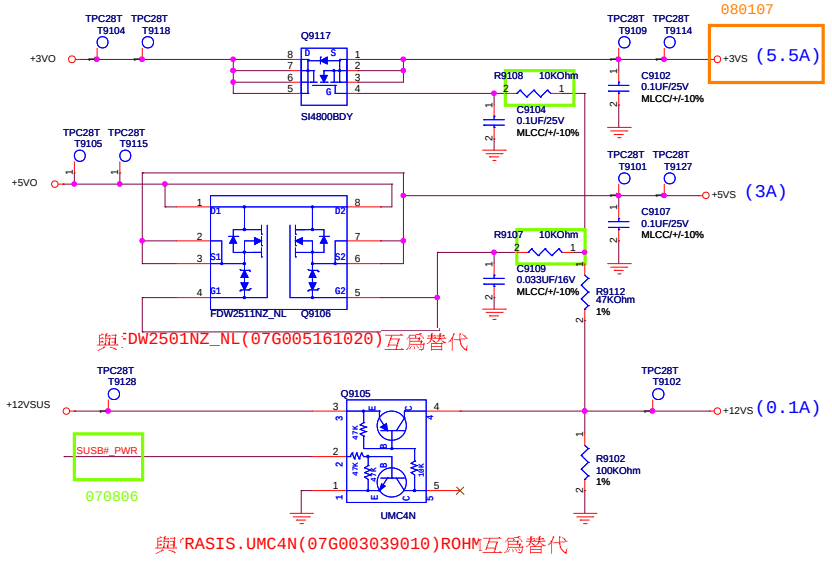


Viinp=Iinput*RS*Glinp*R8807
Viinp=1.877V, RS=20mohm,
Glinp=2.8uA/mV,Pinput=63.65W

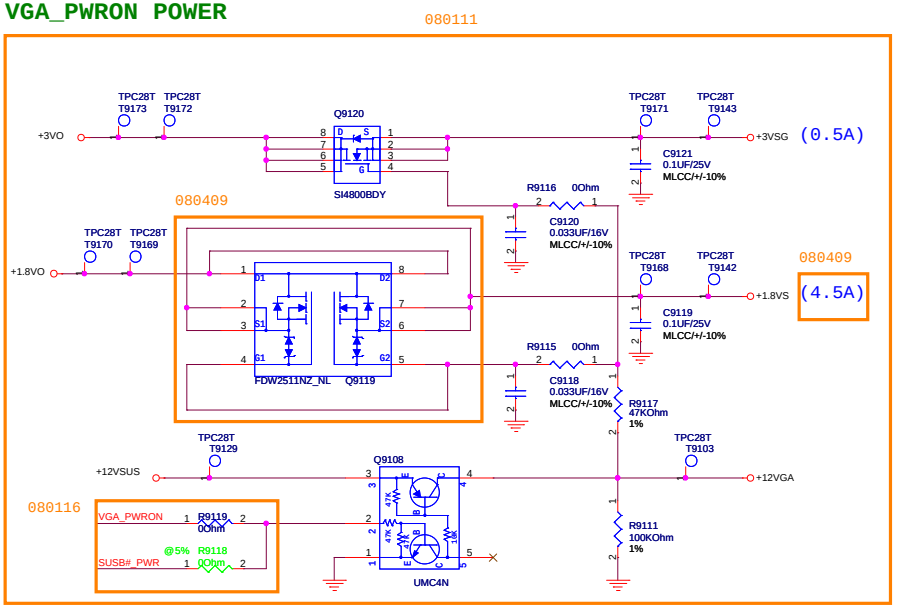
R8839=10K----->Iinput=3.35A

ASUSTeK COMPUTER INC	Title : POWER_DETECT	
	Engineer: Benson	
Size: Custom	Project Name: N10	Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 90 of 97	

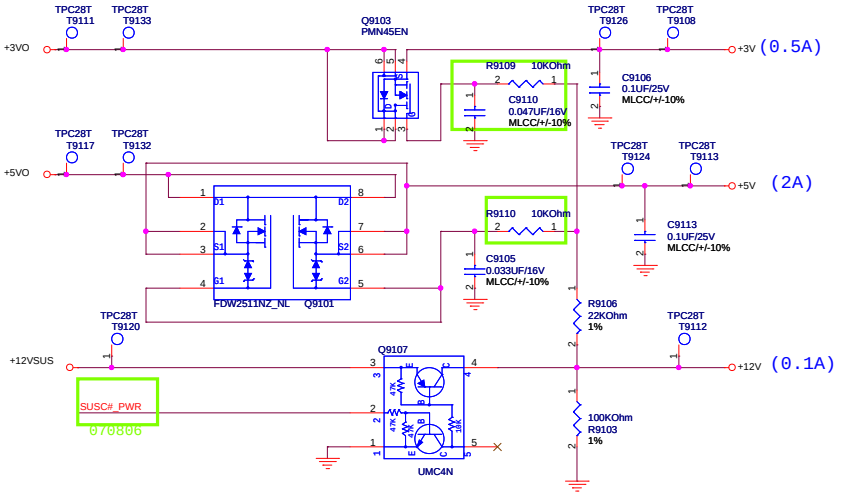
SUSB#_PWR POWER

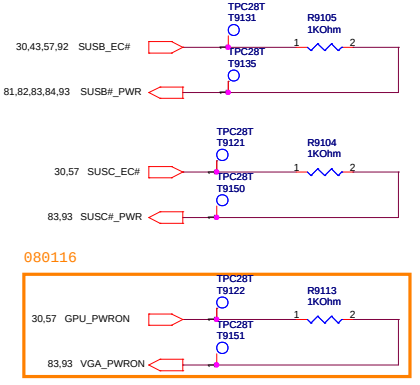


VGA_PWRON POWER



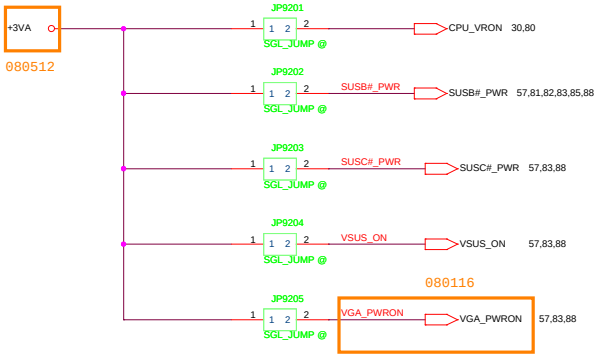
SUSC#_PWR POWER



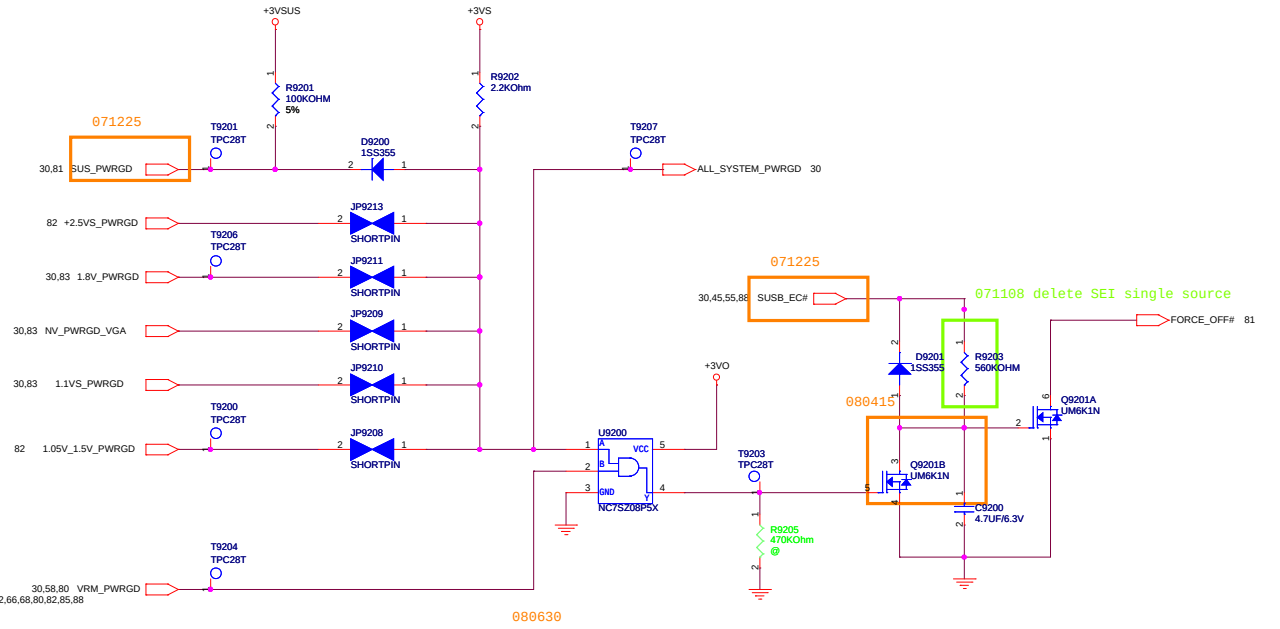


ASUSTeK COMPUTER INC	Title : POWER LOAD SWITCH	
	Engineer: Benson	
Size: Custom	Project Name: N10	Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 91 of 97	

FOR POWER TEST



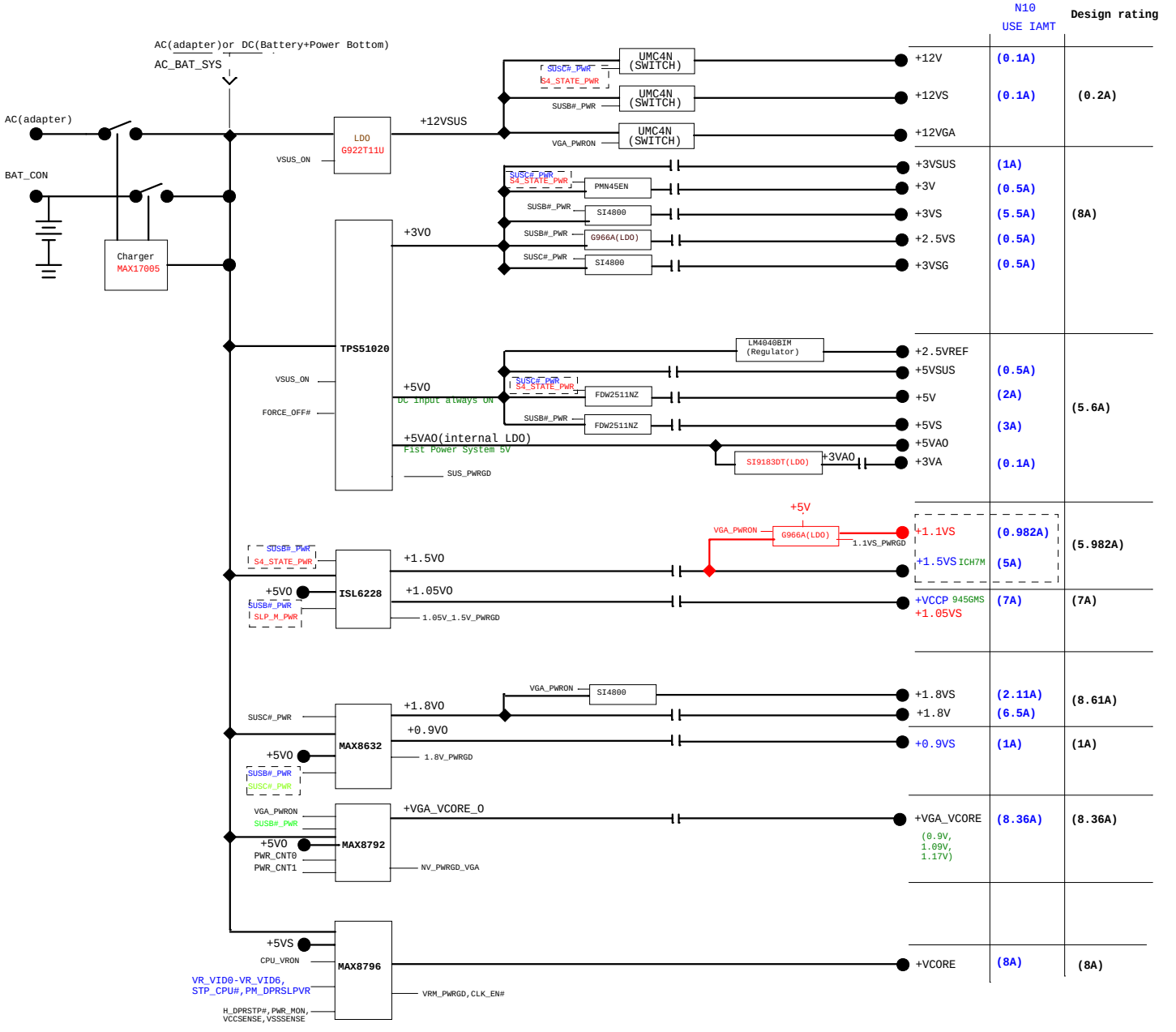
POWER GOOD DETECTER



AC_BAT_SYS	AC_BAT_SYS	80,81,82,83,84
BAT	BAT	60,84
BAT_CON	BAT_CON	60,84
+3VA	+3VA	12,30,57,85,86
+5VO	+5VO	81,82,83,85,88
+5VSUS	+5VSUS	56,62,81
+3VO	+3VO	53,81,88
+3VSUS	+3VSUS	30,37,81
+5V	+5V	9,14,39,52,56,57,65,69,88
+5VS	+5VS	14,36,37,45,48,50,56,57,61,62,69,80,82,88
+3V	+3V	13,14,30,45,52,54,57,62,65,88
+3VS	+3VS	7,12,13,14,29,30,35,36,37,42,44,45,48,50,51,53,54,55,56,57,58,61,62,66,68,80,82,85,88
+12V	+12V	48,57,66,81
+12VS	+12VS	48,57,66,81
+2.5VS	+2.5VS	48,57,66,81
+1.8VO	+1.8VO	83
+1.8V	+1.8V	7,9,11,14,57,83,85
+1.8VS	+1.8VS	7,9,11,14,57,83,85
+0.9VS	+0.9VS	7,9,11,83
+VCCP	+VCCP	4,10,13,14,29,53,57,85
+1.05VO	+1.05VO	82
+1.5VS	+1.5VS	4,10,13,14,29,53,57,85
+VCORE	+VCORE	4,80
+VGA_Vcore	+VGA_Vcore	4,10,13,14,29,53,57,85
+1.1VS	+1.1VS	60,84
GPU_VID0	GPU_VID0	60,84
GPU_VID1	GPU_VID1	60,84
NVDD_SENSE	NVDD_SENSE	60,84

R2.0 080331 Add Q9201, R9204 and un-mount U9200 for cost down with R9209 change from 100kohm to 10 kohm
080401 Change Q9201 from 2N7002 to BSS138.
080402 Un-Mount Q9201 and R9204, mount U9200. Recover R9209 from 10Kohm to 100Kohm

ASUSTeK COMPUTER INC	Title : Power_PROTECT_SIGNA	Engineer: Benson
Size: Custom	Project Name: N10	Rev: 1.0
Date: Wednesday, July 02, 2008	Sheet 92 of 97	



ASUSTeK COMPUTER INC.

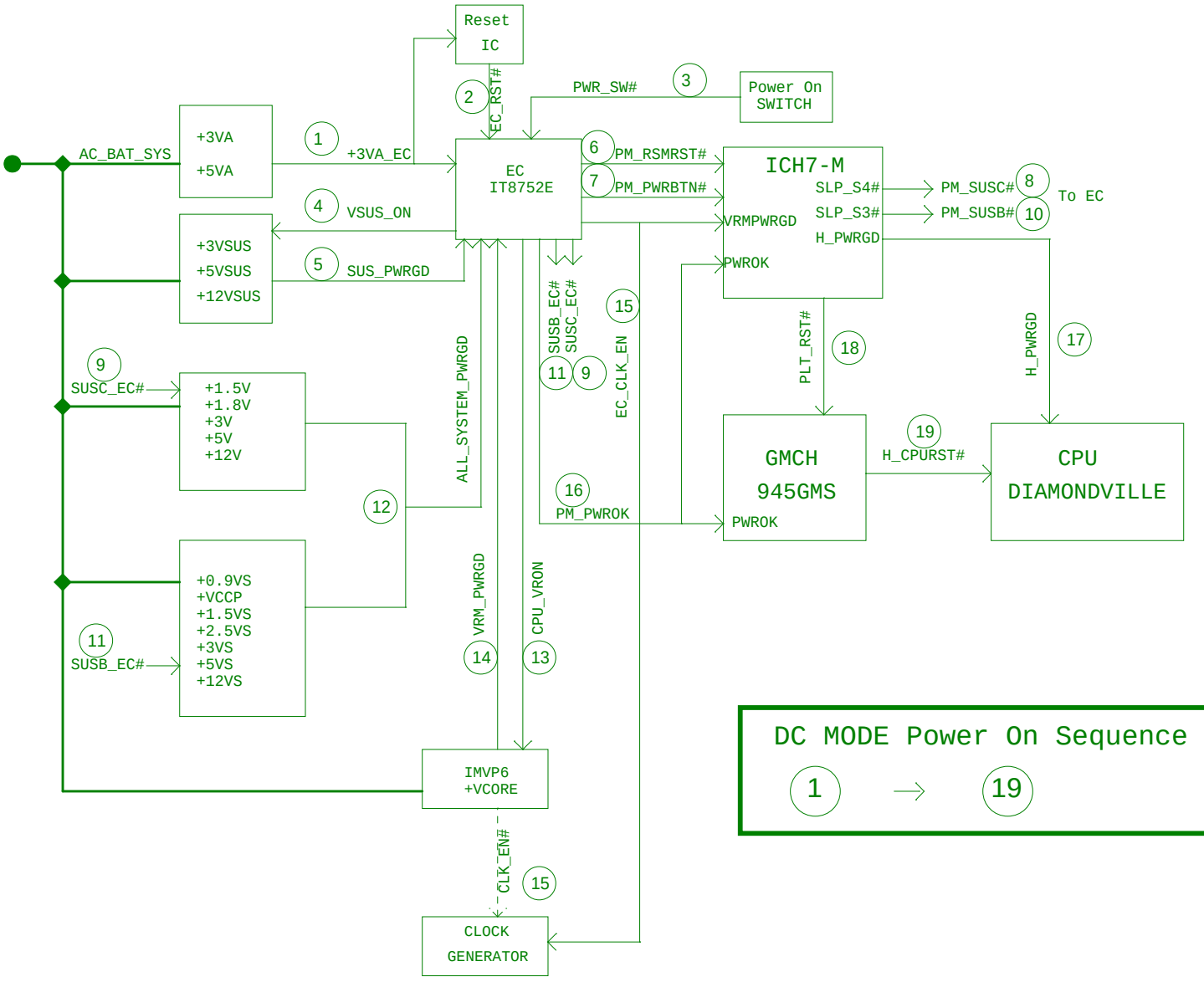
Title : POWER FLOWCHART

Engineer: Benson

Size	Project Name	Rev
Custom	N10	1.0

Date: Wednesday, July 12, 2006 Sheet 93 of 97

N10 POWER-ON SEQUENCE UNDER BATTERY MODE

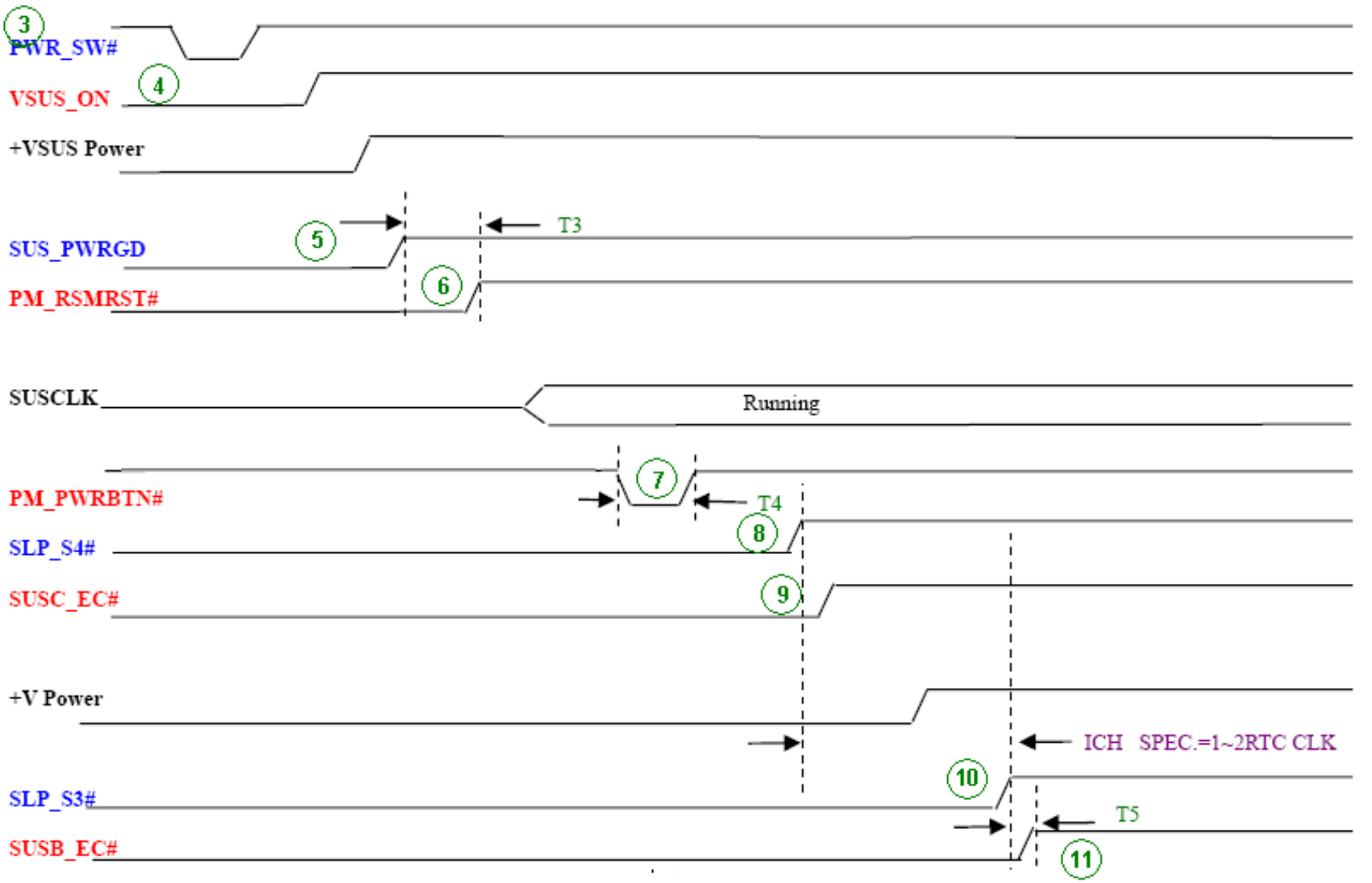


1. Battery is plugged in only and +3VA_EC is on
2. EC_RST# is de-asserted
3. Power button is pressed
4. EC asserts VSUS_ON to turn SUS power on
5. SUS_PWRGD is asserted to indicate SUS power is OK
6. EC de-asserts PM_RSMRST# to reset RTC well of ICH7M
7. EC asserts PM_PWRBTN# to ICH7M from G2 to G0
8. ICH7M de-asserts PM_SUSC# to EC
9. EC de-asserts SUSC_EC# to turn +V power on
10. ICH7M de-asserts PM_SUSB# to EC
11. EC de-asserts SUSB_EC# to turn +VS power on
12. EC waits for ALL_SYSTEM_PWRGD
13. EC asserts CPU_VRON to turn CPU power on
14. EC waits for VRM_PWRGD
15. EC asserts EC_CLK_EN to enable clock generator
16. EC asserts PM_PWROK to 945GMS and ICH7M
17. ICH7M asserts H_PWRGD to CPU
18. ICH7M asserts PLT_RST# to reset 945GMS
19. 945GMS asserts H_CPURST# to reset CPU

DC MODE Power On Sequence

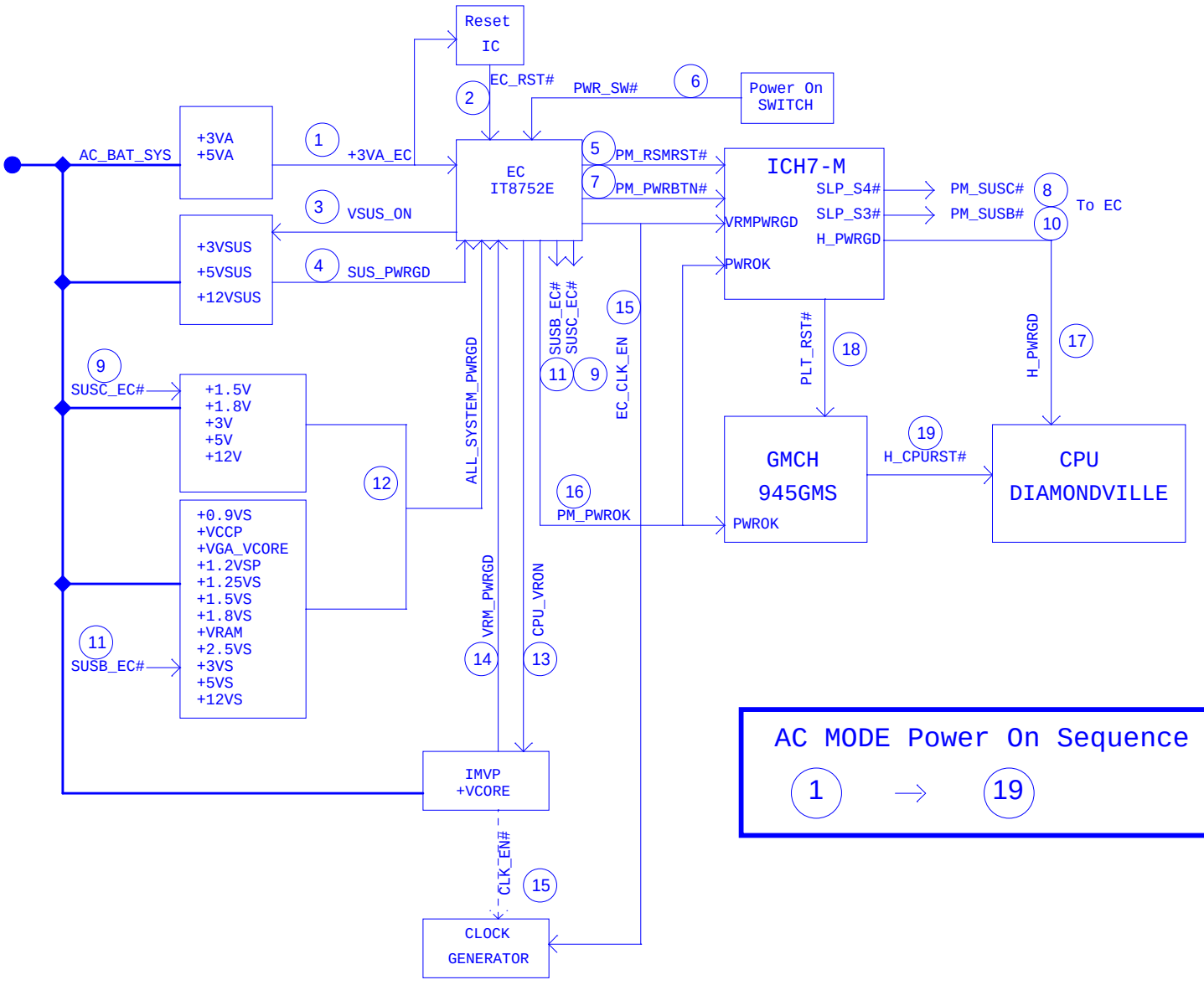
1 → 19

ASUSTeK COMPUTER INC	Title : POWER ON SEQUENCE(1)	Engineer: ENGINEER
Size C	Project Name N10	Rev 0.1
Date: Wednesday, July 02, 2008	Sheet 94 of 97	



ASUSTeK COMPUTER INC	Title : POWER ON SEQUENCE(1)	Engineer: ENGINEER
Size: A	Project Name: N10	Rev: 0.1
Date: Wednesday, July 02, 2008	Sheet 95 of 97	

N10 POWER-ON SEQUENCE UNDER BATTERY MODE

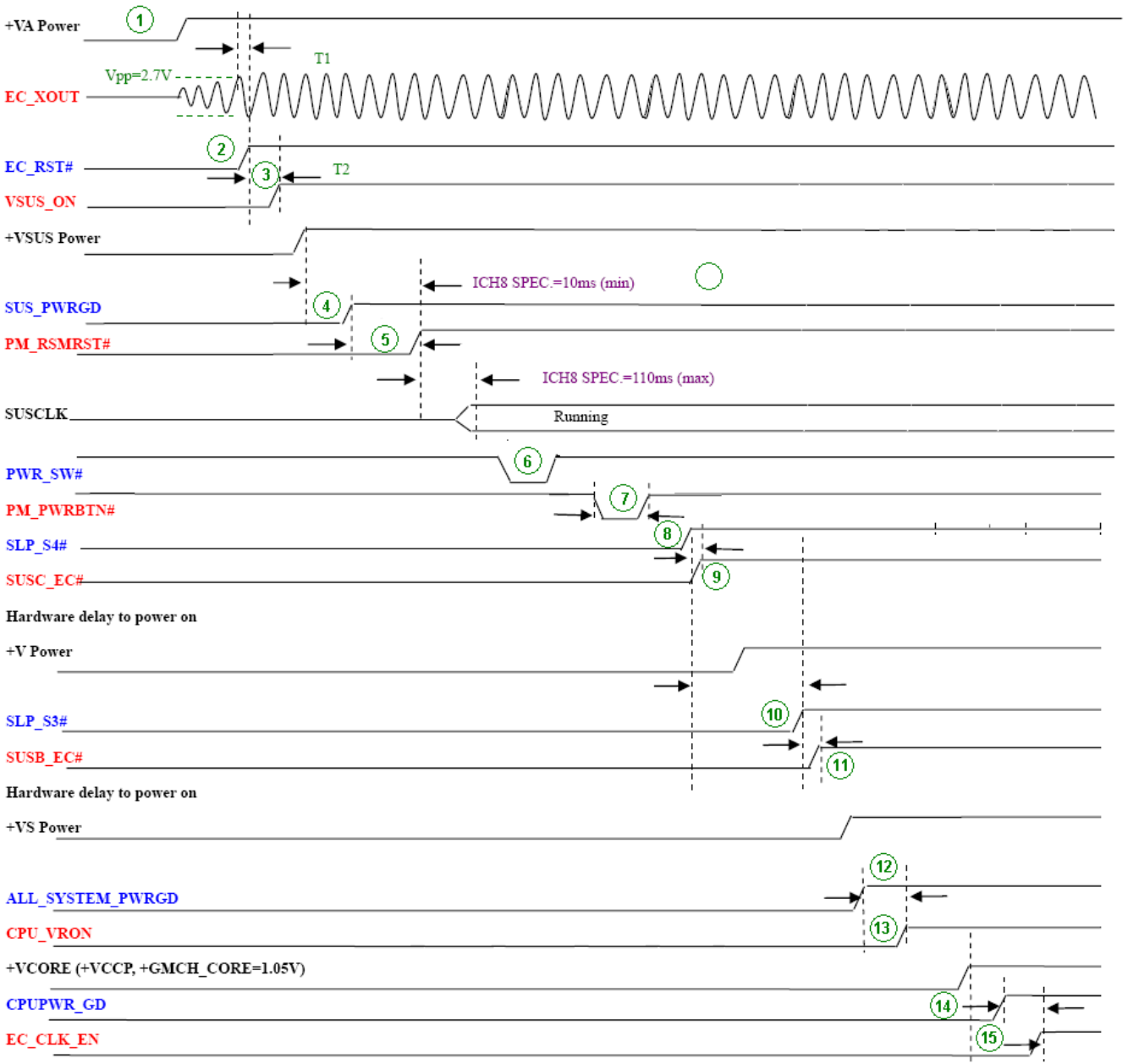


1. Battery is plugged in only and +3VA_EC is on
2. EC_RST# is de-asserted
3. Power button is pressed
4. EC asserts VSUS_ON to turn SUS power on
5. SUS_PWRGD is asserted to indicate SUS power is OK
6. EC de-asserts PM_RSMRST# to reset RTC well of ICH7M
7. EC asserts PM_PWRBTN# to ICH7M from G2 to G0
8. ICH7M de-asserts PM_SUSC# to EC
9. EC de-asserts SUSC_EC# to turn +V power on
10. ICH7M de-asserts PM_SUSB# to EC
11. EC de-asserts SUSB_EC# to turn +VS power on
12. EC waits for ALL_SYSTEM_PWRGD
13. EC asserts CPU_VRON to turn CPU power on
14. EC waits for VRM_PWRGD
15. EC asserts EC_CLK_EN to enable clock generator
16. EC asserts PM_PWROK to 945GMS and ICH7M
17. ICH7M asserts H_PWRGD to CPU
18. ICH7M asserts PLT_RST# to reset 945GMS
19. 945GMS asserts H_CPURST# to reset CPU

AC MODE Power On Sequence

1 → 19

ASUSTeK COMPUTER INC	Title : POWER ON SEQUENCE(1)	
	Engineer: ENGINEER	
Size: C	Project Name: N10	Rev: 0.1
Date: Wednesday, July 02, 2008	Sheet 96 of 97	



ASUSTeK COMPUTER INC	Title : POWER ON SEQUENCE(1)	Engineer: ENGINEER
Size: B	Project Name: N10	Rev: 0.1
Date: Wednesday, July 02, 2008	Sheet 97 of 97	