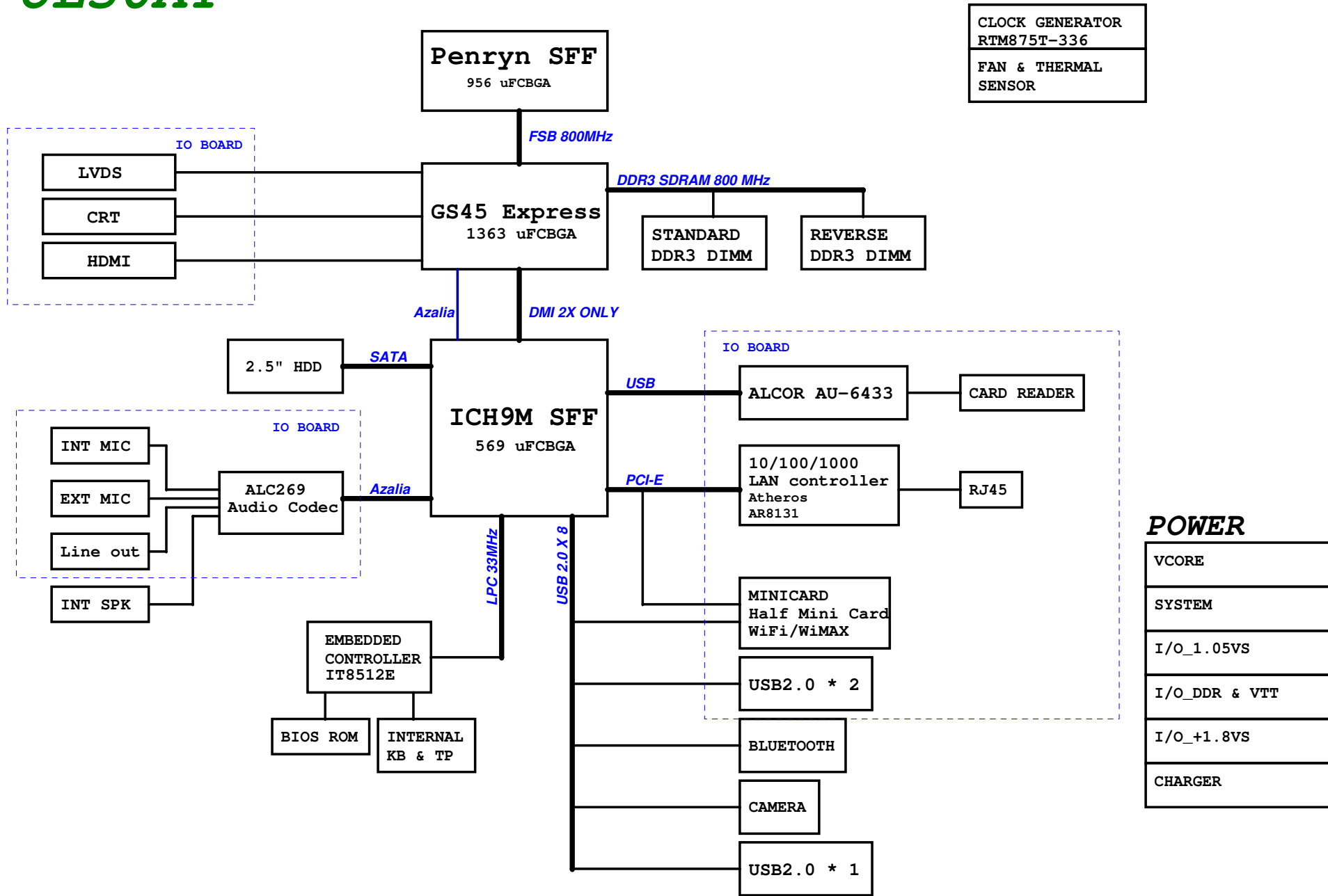


UL50AT



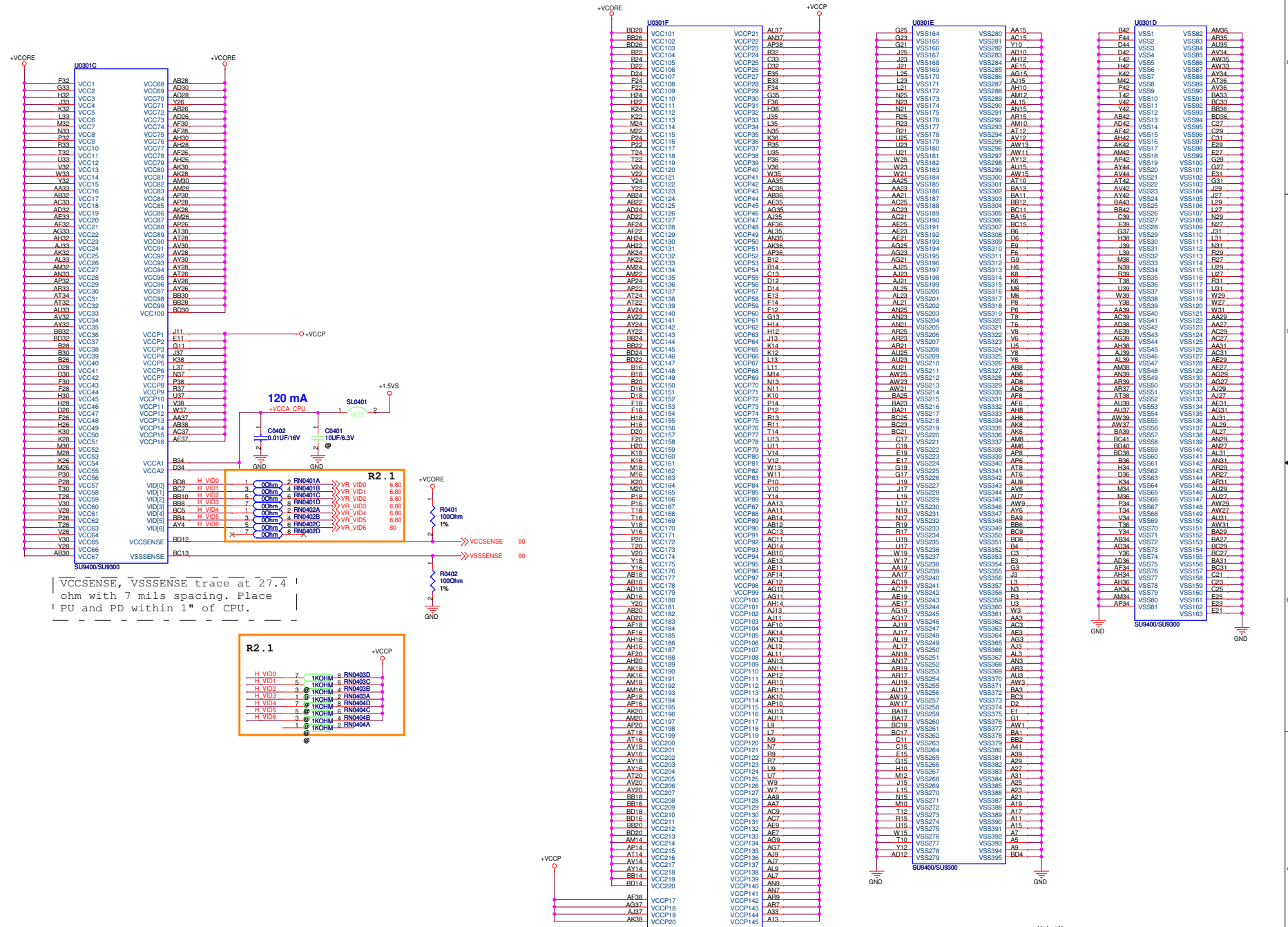
CLOCK GENERATOR
RTM875T-336

FAN & THERMAL
SENSOR

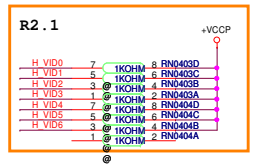
POWER

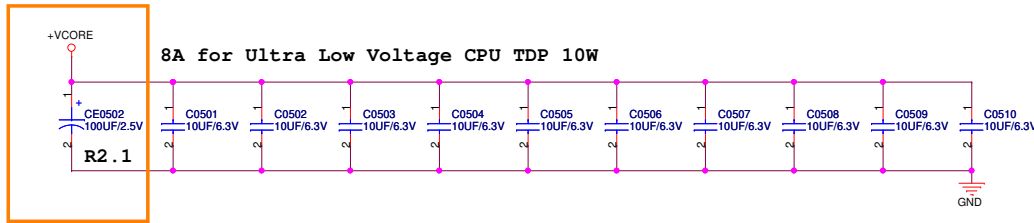
VCORE
SYSTEM
I/O_1.05VS
I/O_DDR & VTT
I/O_+1.8VS
CHARGER

<Variant Name>



VCCSENSE, VSSSENSE trace at 27.4 ohm with 7 mils spacing. Place PU and PD within 1" of CPU.

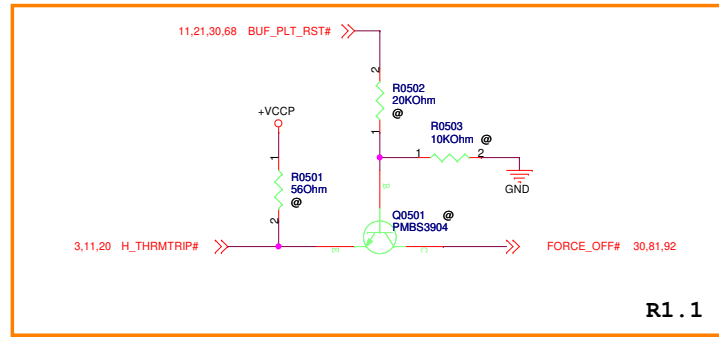
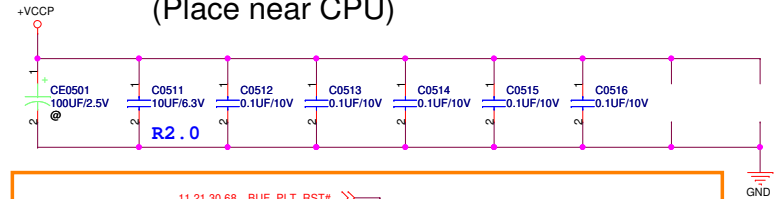


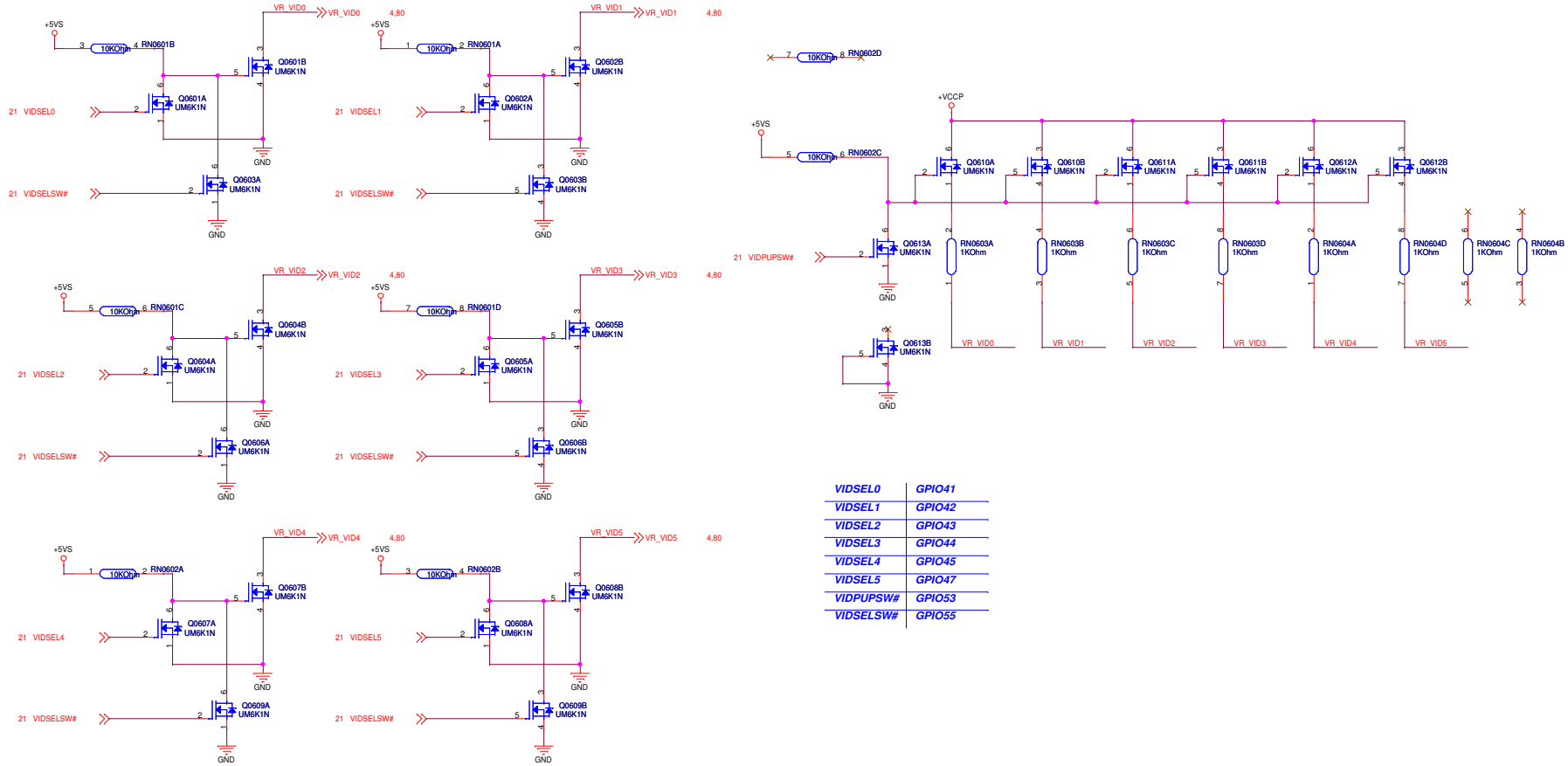


Decoupling guide from Intel

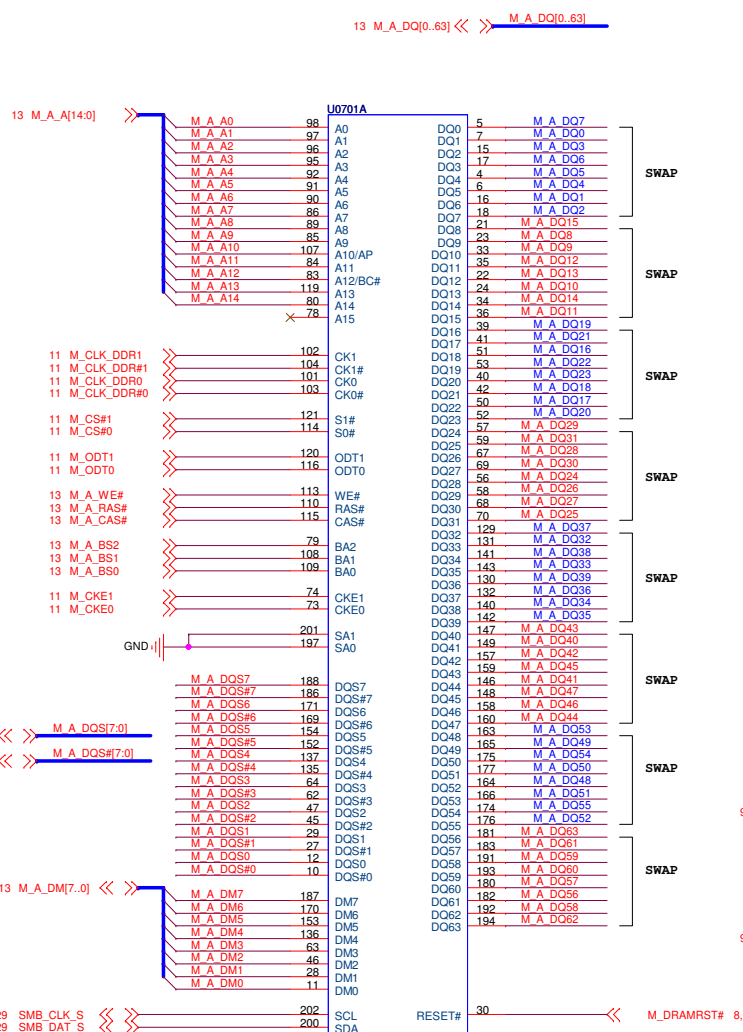
V CORE	10uF mount	*4pcs
	0.1uF mount	*5pcs
V CCP	1uF	* 12pcs
	270uF	* 1pcs
V CCA	0.01uF	* 1 pcs
	10uF	* 1 pcs

**+VCCP Decoupling Capacitor
(Place near CPU)**

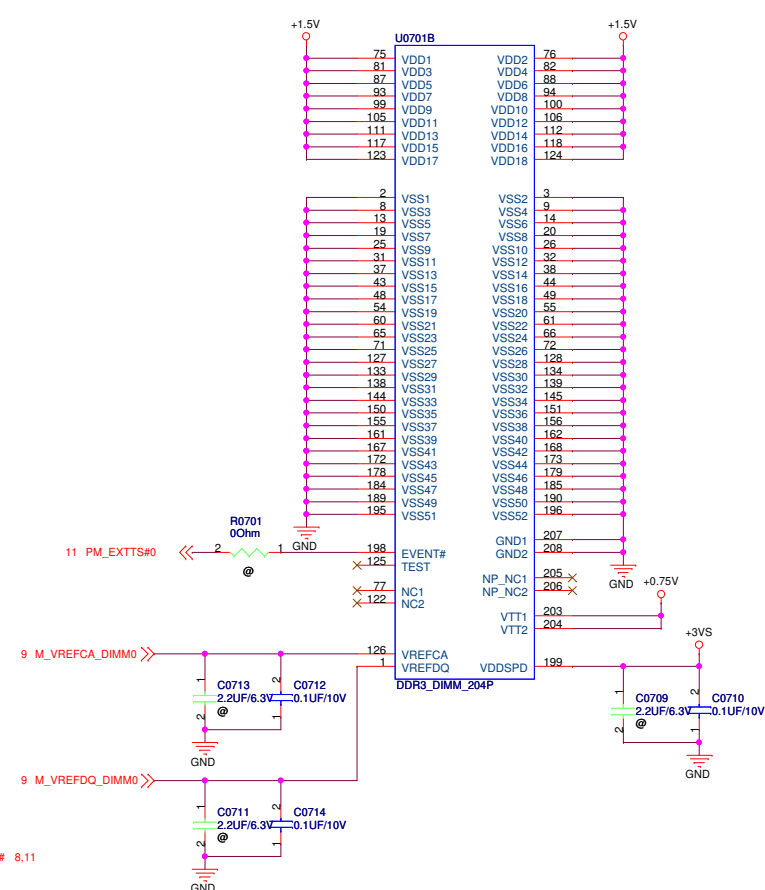
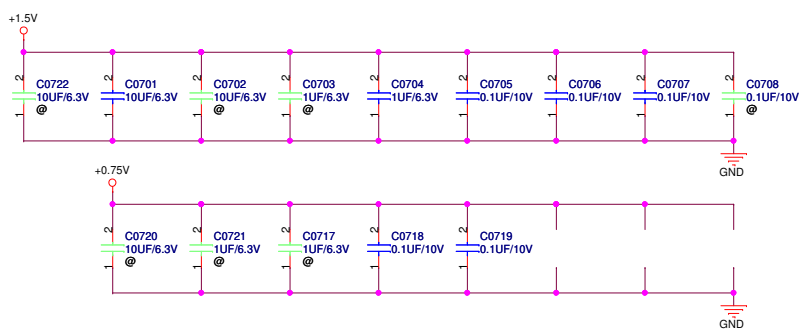
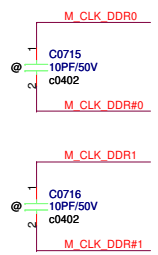




VIDSEL0	GPIO41
VIDSEL1	GPIO42
VIDSEL2	GPIO43
VIDSEL3	GPIO44
VIDSEL4	GPIO45
VIDSEL5	GPIO47
VIDPUPSW#	GPIO53
VIDSEL5#	GPIO55

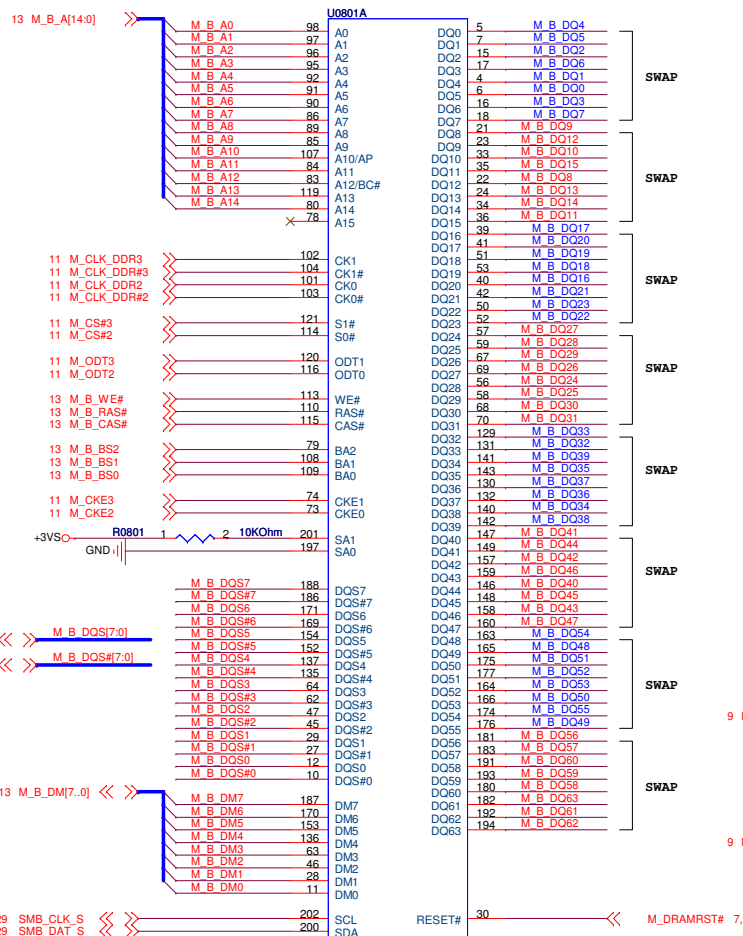
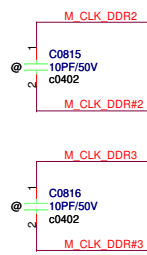


Place near SO-DIMM_0

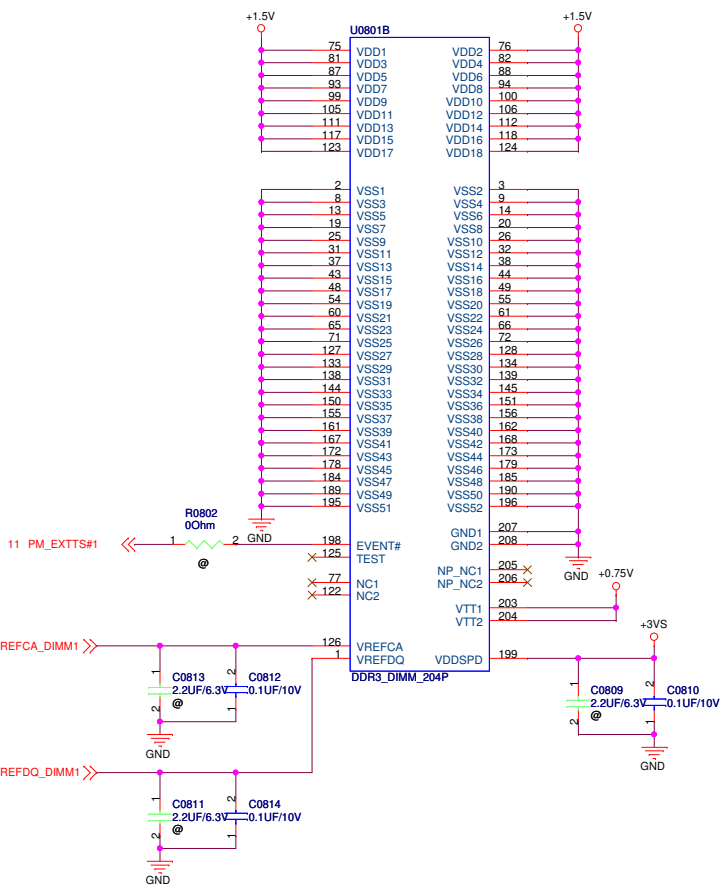
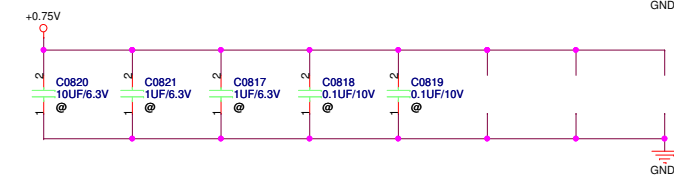
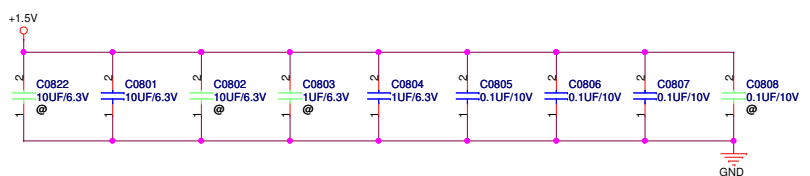


DDR3 DIMM_204P
12G02553204W
DDR3 DIMM 204P,1.5V,5.2H,REV

Place near SO-DIMM_1



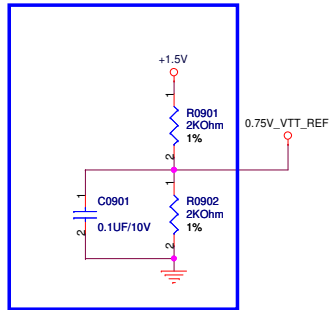
DDR3 DIMM_204P
12G02553204K
DDR3 DIMM 204P,1.5V,5.2H,STD



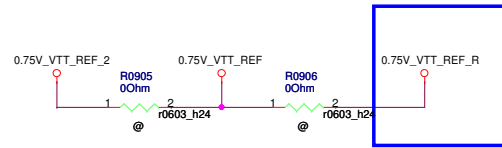
<Variant Name>

ASUS		Title : DDR3 SO-DIMM B	
ASUSTek COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	8 of 97

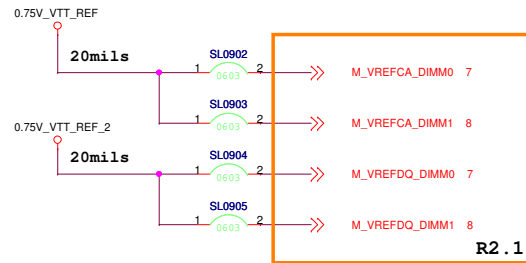
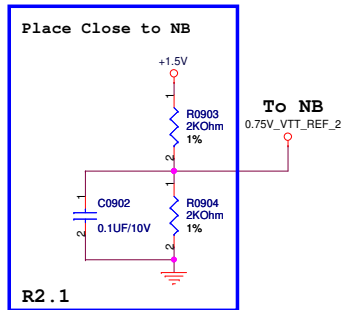
R2.1

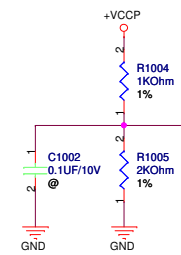
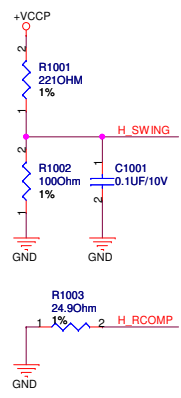


From DDR/VTT Power Circuit



Place Close to NB





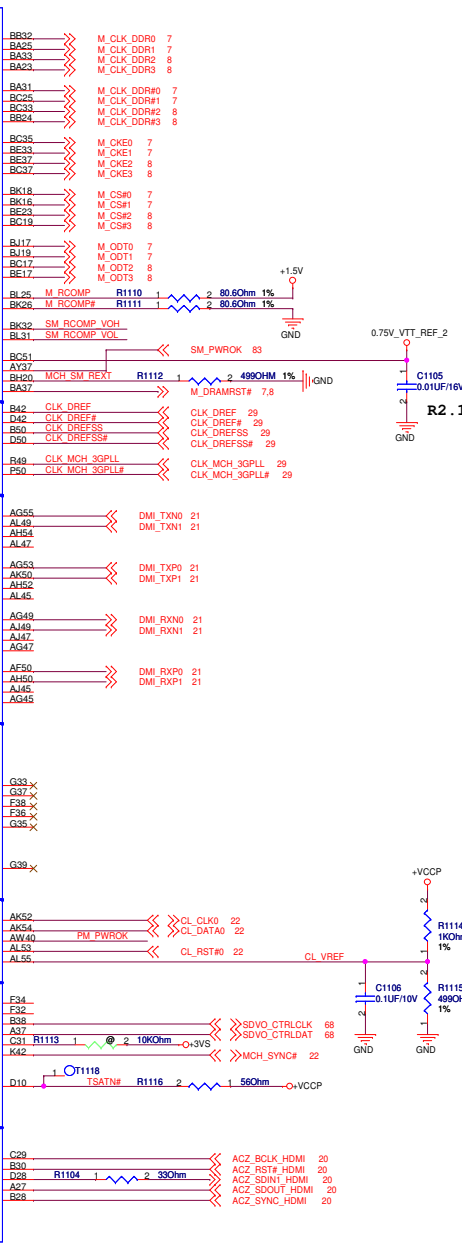
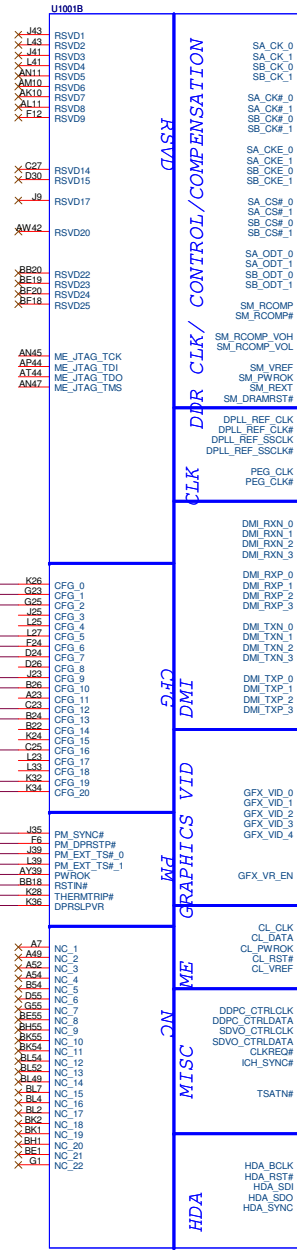
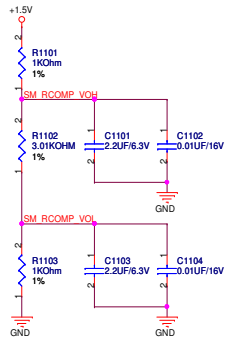
3 H_A#[35:3] <<>> H_A#[35:3]
 3 H_REQ#[4:0] <<>> H_REQ#[4:0]
 3 H_D#[63:0] <<>> H_D#[63:0]

U1001A		
H_D#0	J7	H_D#_0
H_D#1	H6	H_D#_1
H_D#2	L11	H_D#_2
H_D#3	J3	H_D#_3
H_D#4	H4	H_D#_4
H_D#5	G3	H_D#_5
H_D#6	K10	H_D#_6
H_D#7	K12	H_D#_7
H_D#8	L1	H_D#_8
H_D#9	M10	H_D#_9
H_D#10	M6	H_D#_10
H_D#11	L7	H_D#_11
H_D#12	N11	H_D#_12
H_D#13	K6	H_D#_13
H_D#14	M4	H_D#_14
H_D#15	K4	H_D#_15
H_D#16	P6	H_D#_16
H_D#17	W9	H_D#_17
H_D#18	V6	H_D#_18
H_D#19	V2	H_D#_19
H_D#20	P10	H_D#_20
H_D#21	W7	H_D#_21
H_D#22	N6	H_D#_22
H_D#23	P4	H_D#_23
H_D#24	U9	H_D#_24
H_D#25	V4	H_D#_25
H_D#26	U1	H_D#_26
H_D#27	W3	H_D#_27
H_D#28	V10	H_D#_28
H_D#29	U7	H_D#_29
H_D#30	W11	H_D#_30
H_D#31	L11	H_D#_31
H_D#32	AC11	H_D#_32
H_D#33	AC9	H_D#_33
H_D#34	Y4	H_D#_34
H_D#35	Y10	H_D#_35
H_D#36	AB6	H_D#_36
H_D#37	AA9	H_D#_37
H_D#38	AB10	H_D#_38
H_D#39	AA1	H_D#_39
H_D#40	AC3	H_D#_40
H_D#41	AC7	H_D#_41
H_D#42	AD12	H_D#_42
H_D#43	AB4	H_D#_43
H_D#44	Y6	H_D#_44
H_D#45	AD10	H_D#_45
H_D#46	AA11	H_D#_46
H_D#47	AB2	H_D#_47
H_D#48	AD4	H_D#_48
H_D#49	AE7	H_D#_49
H_D#50	AD2	H_D#_50
H_D#51	AD6	H_D#_51
H_D#52	AE3	H_D#_52
H_D#53	AG9	H_D#_53
H_D#54	AG7	H_D#_54
H_D#55	AE11	H_D#_55
H_D#56	AK6	H_D#_56
H_D#57	AE6	H_D#_57
H_D#58	AJ9	H_D#_58
H_D#59	AH6	H_D#_59
H_D#60	AF12	H_D#_60
H_D#61	AH4	H_D#_61
H_D#62	AJ7	H_D#_62
H_D#63	AE9	H_D#_63
H_SWING	B6	H_SWING
H_RCOMP	D4	H_RCOMP
H_CPURST#	J11	H_CPURST#
H_CPUSLP#	G9	H_CPUSLP#
H_AVREF	L17	H_AVREF
H_DVREF	K18	H_DVREF

HOST

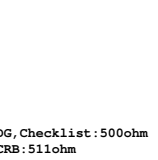
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H_A#_4	B14	H_A#4
H_A#_5	C15	H_A#5
H_A#_6	D12	H_A#6
H_A#_7	F14	H_A#7
H_A#_8	G17	H_A#8
H_A#_9	B12	H_A#9
H_A#_10	J15	H_A#10
H_A#_11	D16	H_A#11
H_A#_12	C17	H_A#12
H_A#_13	D14	H_A#13
H_A#_14	F16	H_A#14
H_A#_15	F16	H_A#15
H_A#_16	C21	H_A#16
H_A#_17	D18	H_A#17
H_A#_18	J19	H_A#18
H_A#_19	J21	H_A#19
H_A#_20	B18	H_A#20
H_A#_21	D22	H_A#21
H_A#_22	G19	H_A#22
H_A#_23	J17	H_A#23
H_A#_24	L21	H_A#24
H_A#_25	L19	H_A#25
H_A#_26	G21	H_A#26
H_A#_27	D20	H_A#27
H_A#_28	K22	H_A#28
H_A#_29	F18	H_A#29
H_A#_30	K20	H_A#30
H_A#_31	F20	H_A#31
H_A#_32	F22	H_A#32
H_A#_33	B20	H_A#33
H_A#_34	A19	H_A#34
H_A#_35	A19	H_A#35
H_ADS#	F10	H_ADS# 3
H_ADSTB#_0	A15	H_ADSTB#0 3
H_ADSTB#_1	C19	H_ADSTB#1 3
H_BNR#	B8	H_BNR# 3
H_BPRI#	C11	H_BPRI# 3
H_BREQ#	E5	H_BREQ# 3
H_DBFSY#	D6	H_DBFSY# 3
HPLL_CLK	AJ10	
HPLL_CLK#	AJ11	
H_DPWR#	G11	H_DPWR# 3
H_DRDY#	H2	H_DRDY# 3
H_HIT#	C7	H_HIT# 3
H_HITM#	F8	H_HITM# 3
H_LOCK#	A11	H_LOCK# 3
H_TRDY#	D8	H_TRDY# 3
H_DIN#_0	L9	H_DIN#0 3
H_DIN#_1	N7	H_DIN#1 3
H_DIN#_2	AA7	H_DIN#2 3
H_DIN#_3	AG3	H_DIN#3 3
H_DSTBN#_0	K2	H_DSTBN#0 3
H_DSTBN#_1	N3	H_DSTBN#1 3
H_DSTBN#_2	AA3	H_DSTBN#2 3
H_DSTBN#_3	AF4	H_DSTBN#3 3
H_DSTBP#_0	L3	H_DSTBP#0 3
H_DSTBP#_1	M2	H_DSTBP#1 3
H_DSTBP#_2	Y2	H_DSTBP#2 3
H_DSTBP#_3	AF2	H_DSTBP#3 3
H_REQ#_0	J13	H_REQ#0
H_REQ#_1	L13	H_REQ#1
H_REQ#_2	C13	H_REQ#2
H_REQ#_3	G13	H_REQ#3
H_REQ#_4	G15	H_REQ#4
H_RS#_0	F4	H_RS#0 3
H_RS#_1	F2	H_RS#1 3
H_RS#_2	G7	H_RS#2 3

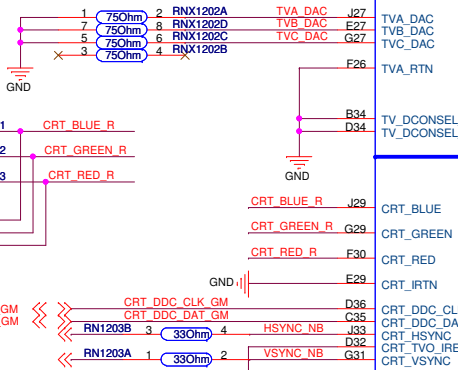
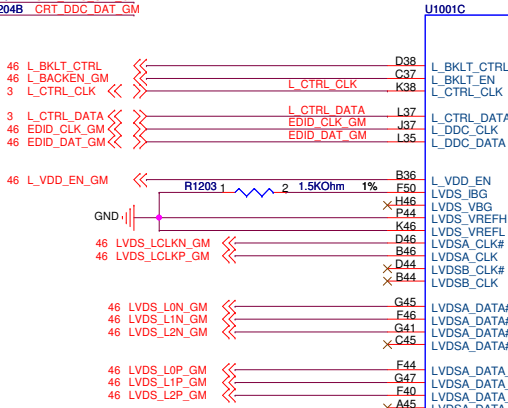
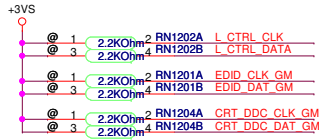




For Clock measurement

CLK_DREF	1	OT1115
CLK_DREF#	1	OT1114
CLK_DREFSS	1	OT1120
CLK_DREFSS#	1	OT1121
CLK_MCH_3GPLL	1	OT1122
CLK_MCH_3GPLL#	1	OT1123

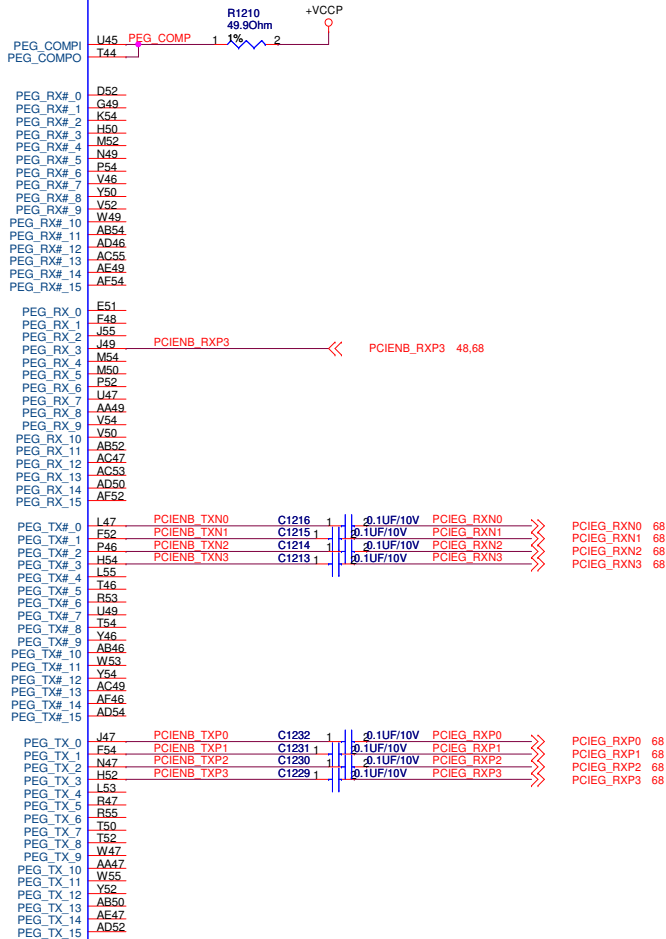




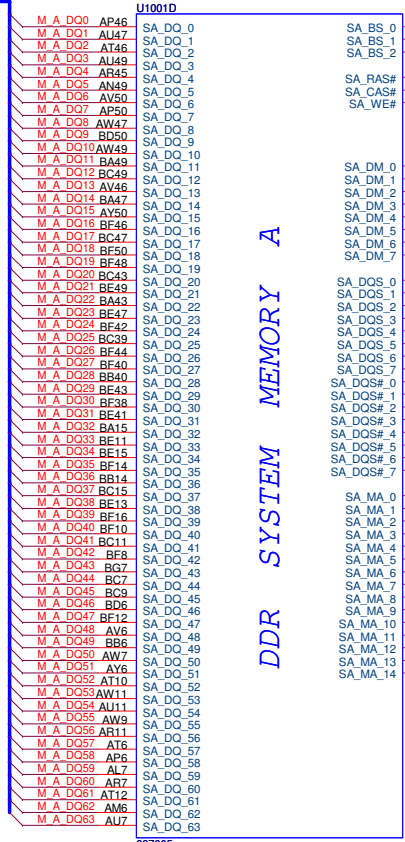
897605

Check : R1208
 如果CRT Trace 12"以内,放1kohm
 如果CRT Trace 12~15.3",放976ohm

PCI-EXPRESS GRAPHICS VGA

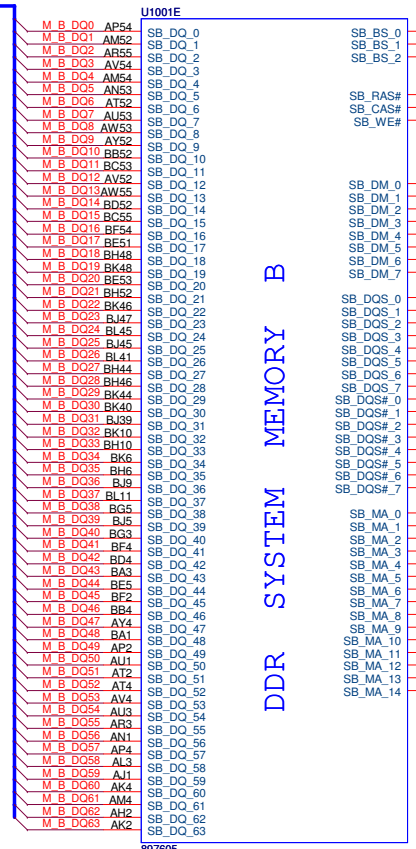


7 M_A_DQ[63:0] << >>



897605

8 M_B_DQ[63:0] << >>

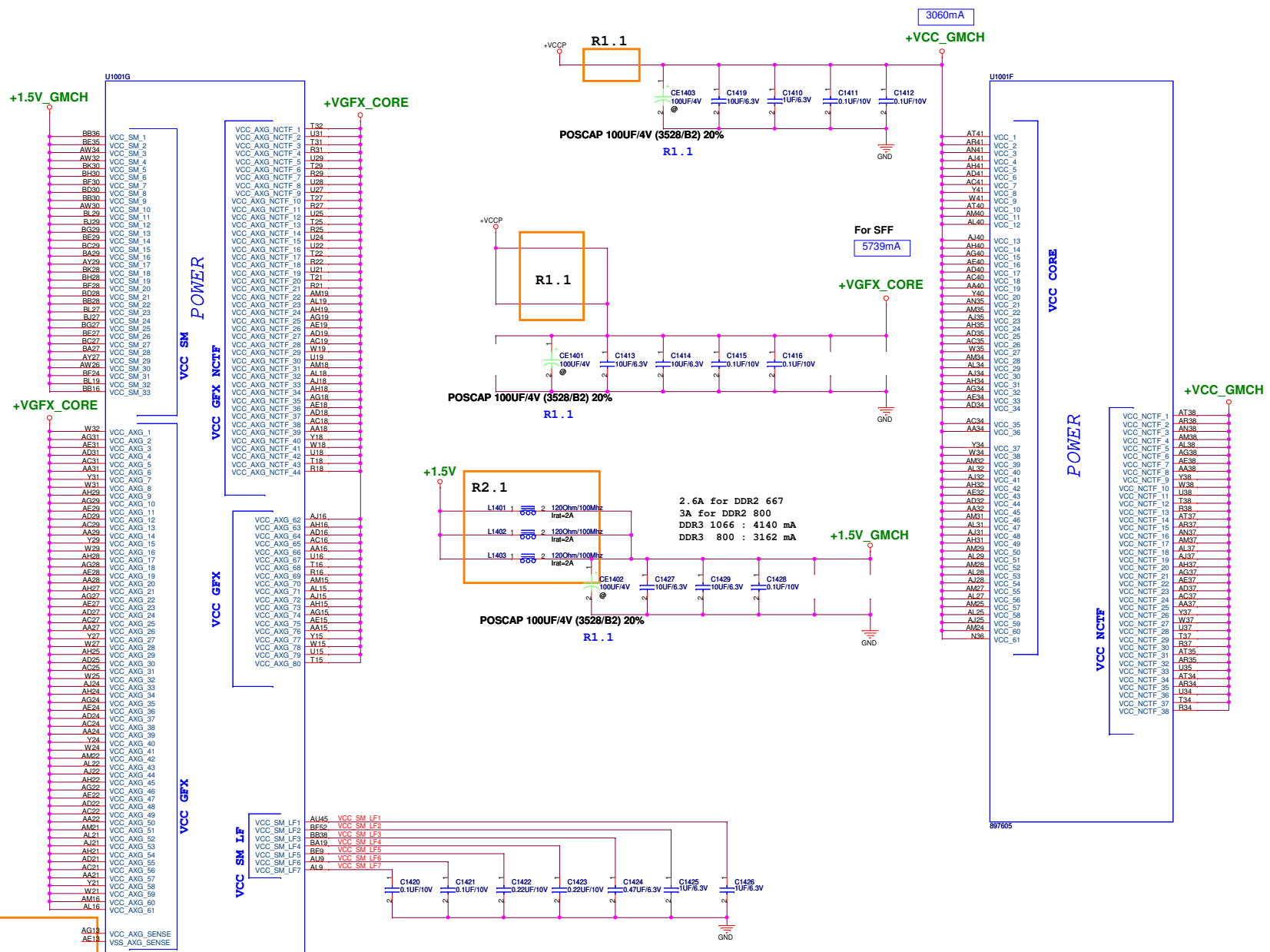


897605

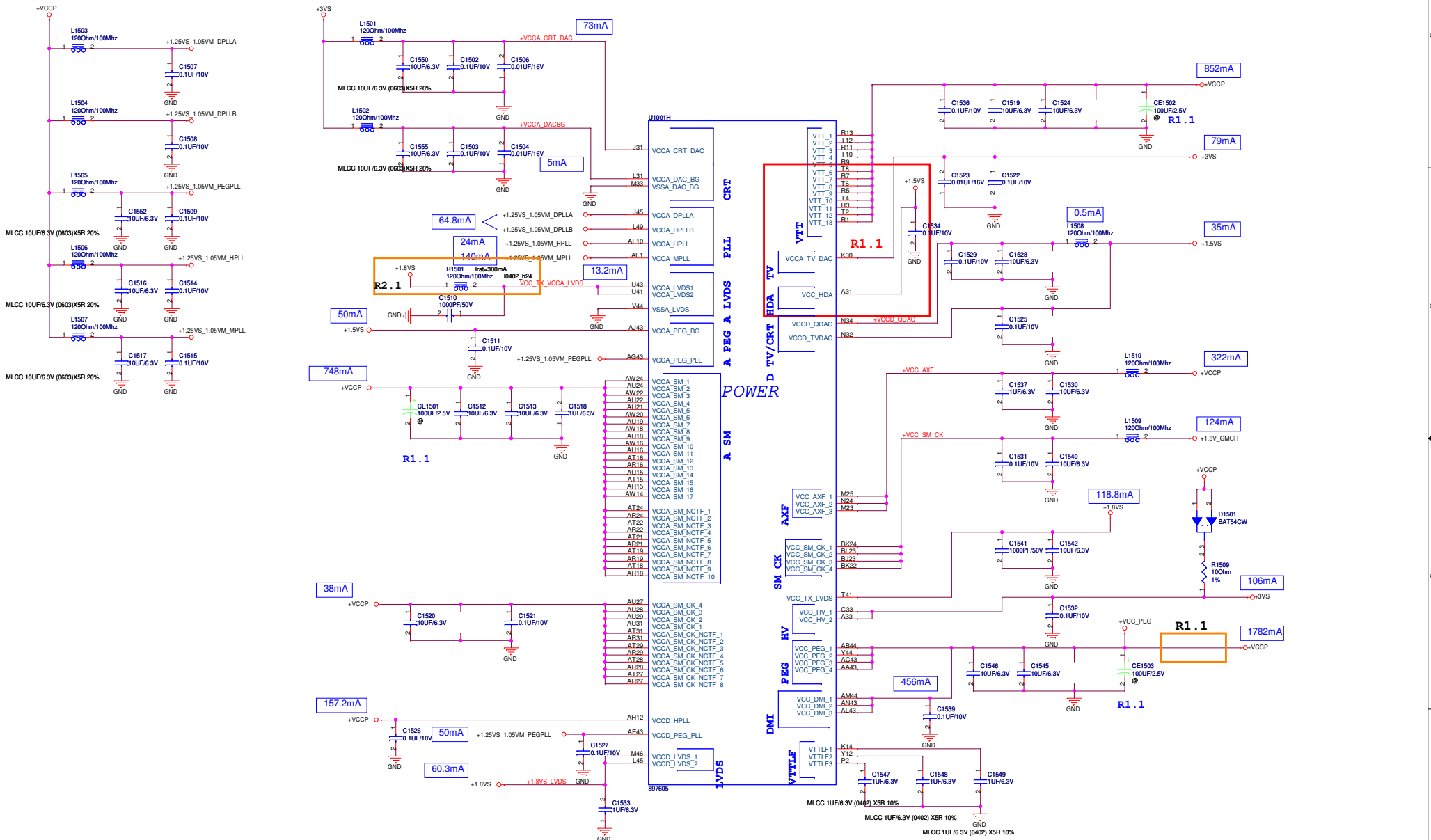
<Variant Name>

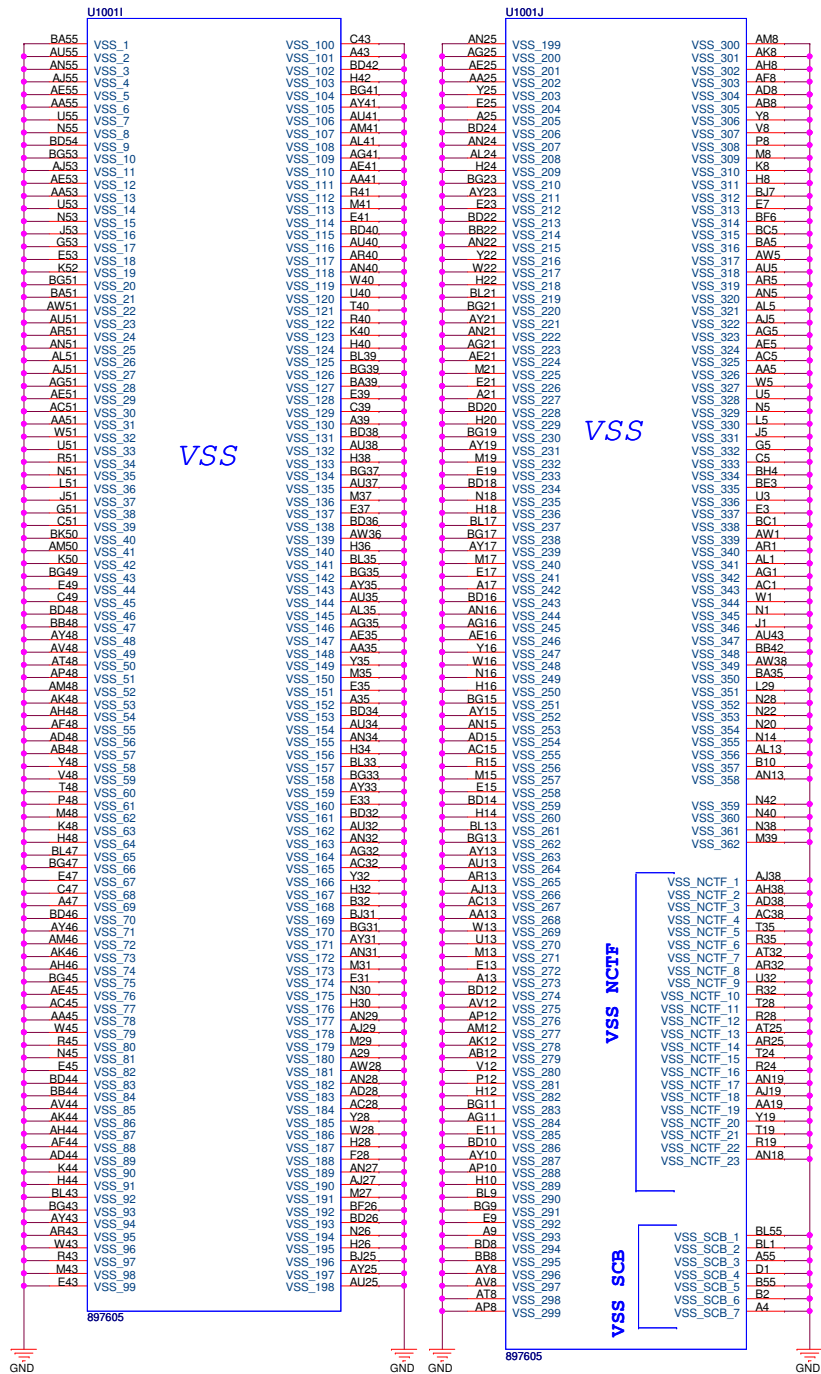
ASUS Title : NB GS45 DDR3 BUS
ASUSTek COMPUTER INC. Engineer: Jack Hsu

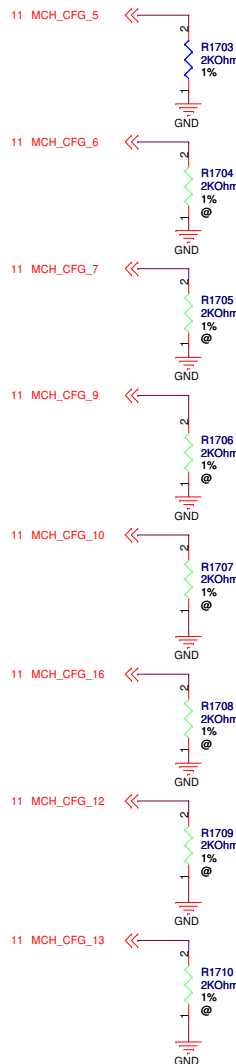
Size	Project Name	Rev
Custom	UL50AT	2.0
Date: Friday, October 16, 2009	Sheet	13 of 97



Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially.







CFG5 : DMI STRAP
H = DMI X 4 (Default)
L = DMI X 2

CFG6 : ITPM Host Interface (Relate to SPI_MOSI)
H = ITPM Disable (Default)
L = ITPM enable(Can disable by SW)

CFG7 : Intel ME Crypto Strap
H = With confidentiality (Default)
L = Without confidentiality

CFG9 : PCIE Graphic Lane Reverse
H = Normal (Default)
L = Lanes Reverse

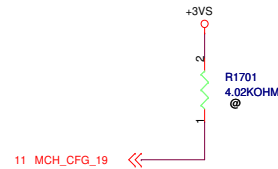
CFG10 : PCIE Loopback
H = Disable (Default)
L = Enable

CFG16 : FSB Dynamic ODT
H =Enable (Default)
L = Disable

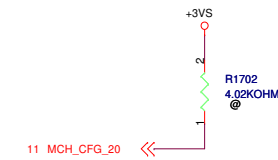
CFG12 : ALL-Z Mode
H =Disable (Default)
L = Enable

CFG13 : XOR Mode
H = Disable (Default)
L = Enable

CFG [13:12] : XOR/ALL-Z
 00 = Reserved
 01= XOR Mode Enabled
 10= All-Z Mode Enabled
11= Normal Operation (Default)



CFG19 : DMI Lane Reversal
H =DMI Lane Reversal
L = Normal (Default)



CFG20 : SDVO/PCIE CONCURRENT MODE
L = Only Digital display port or PCIE is Operational (Default)
H = Digital display port and PCIE are operating simultaneously via the PEG port

<Variant Name>

5

4

3

2

1

D

D

C

C


B

B

A

A

<Variant Name>

		Title :
ASUSTeK COMPUTER INC.		Engineer: <i>Jack Hsu</i>
Size	Project Name	Rev
C	UL50AT	2.0
Date: <u>Friday, October 16, 2009</u>		Sheet 18 of 97

5

4

3

2

1

D

D

C

C


B

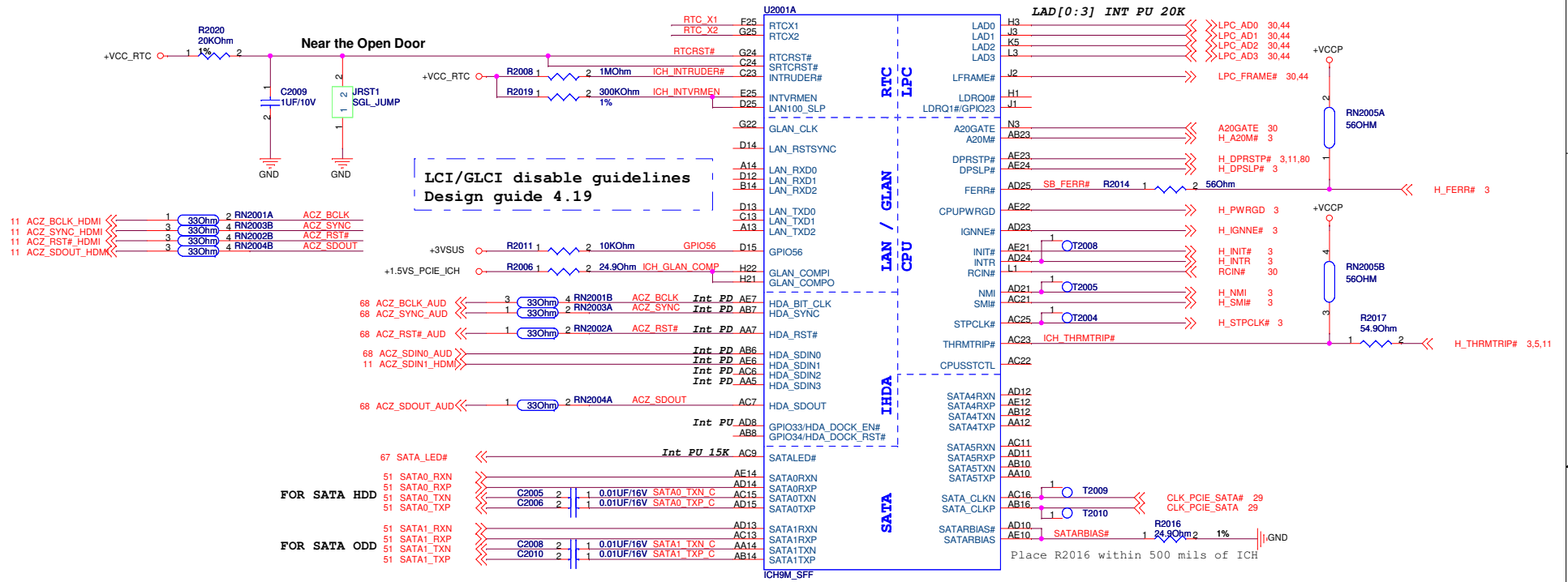
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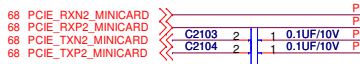
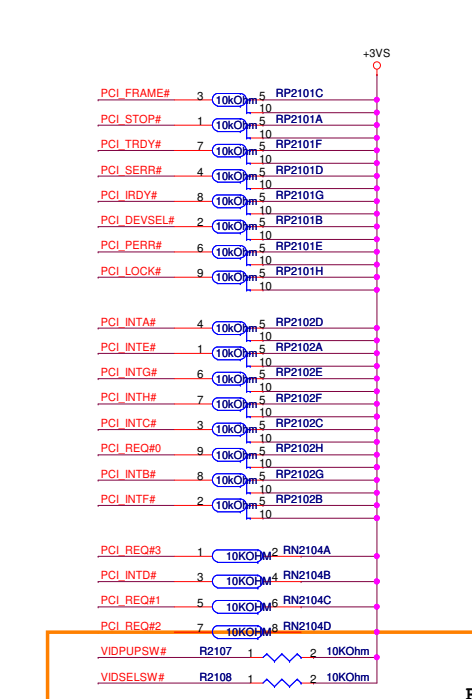
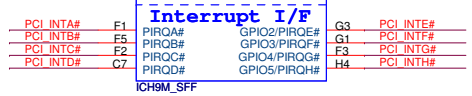
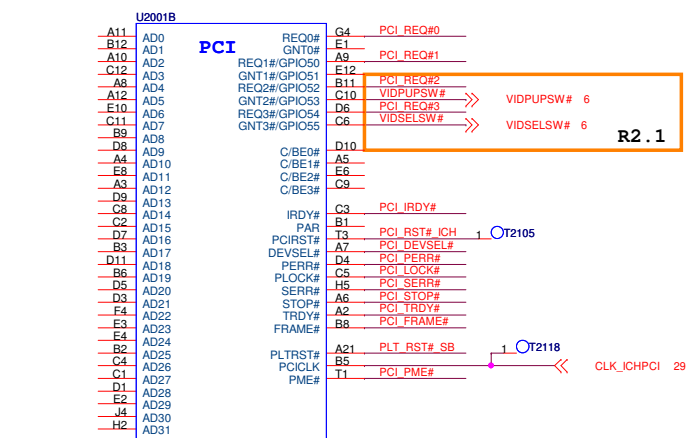
A

A

<Variant Name>

		Title :
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu
Size	Project Name	Rev
C	UL50AT	2.0
Date: Friday, October 16, 2009		Sheet 19 of 97

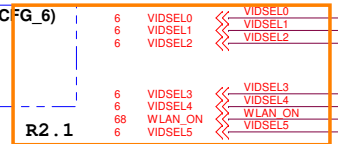




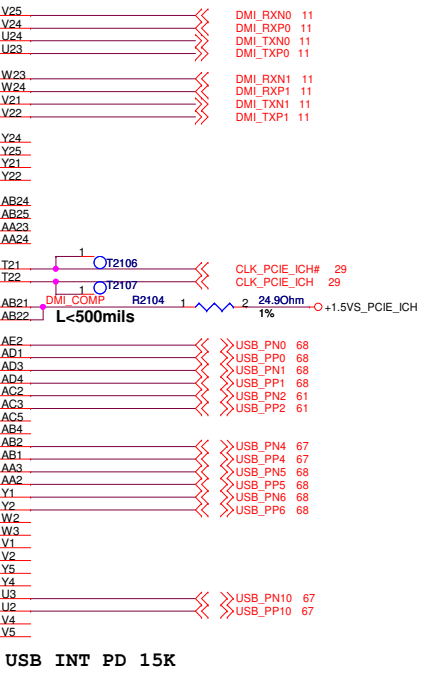
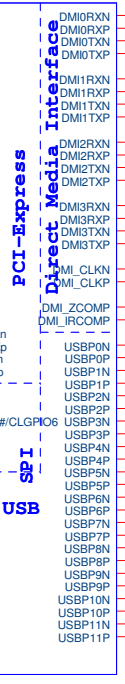
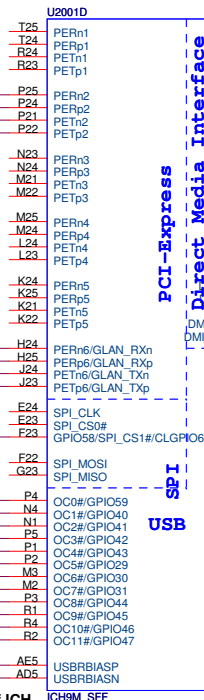
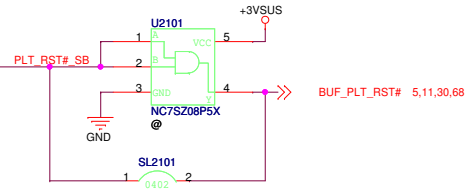
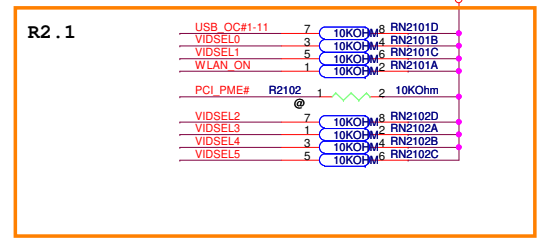
PCIE 1	
PCIE 2	WLAN
PCIE 3	
PCIE 4	
PCIE 5	
PCIE 6	GLAN



SPI_MOSI (relate to MCH_CFG_6)
 iTPM Enable
 H: Enable
 L: Disable(Default)



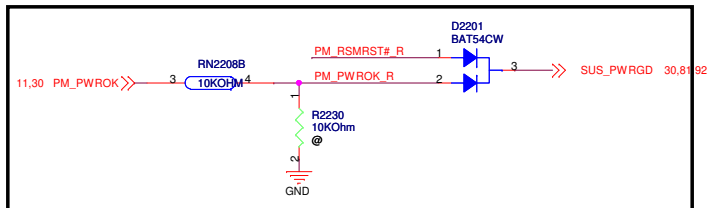
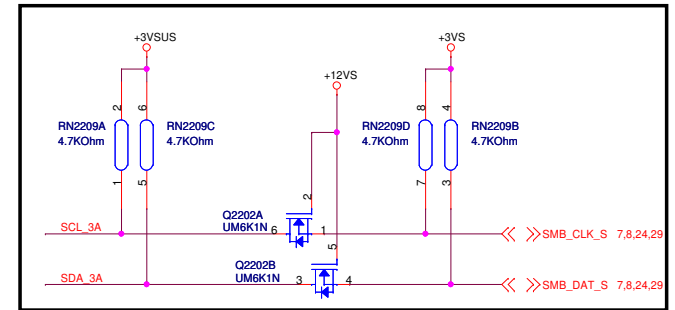
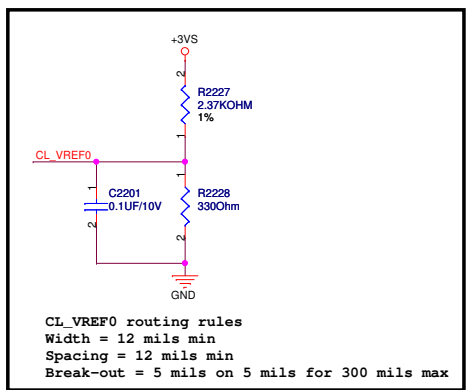
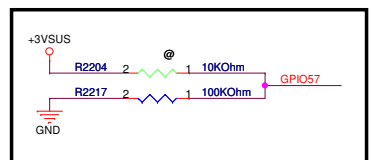
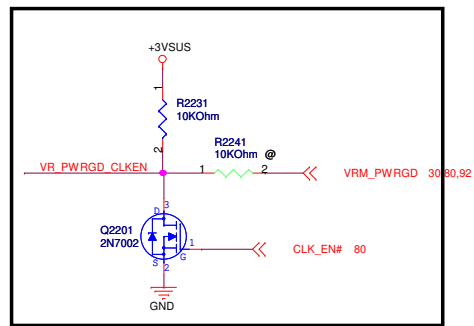
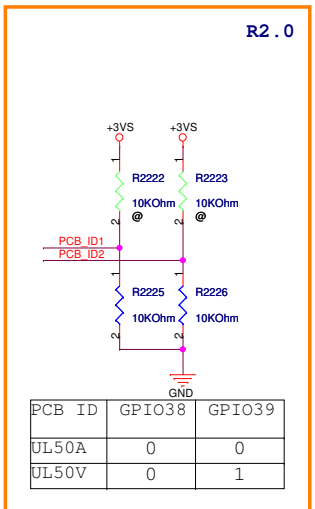
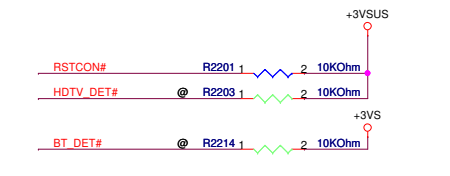
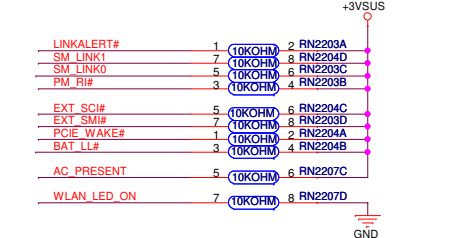
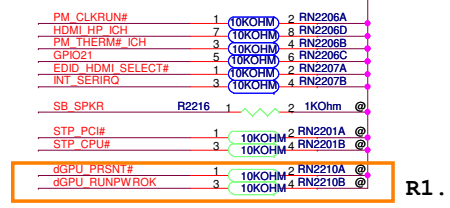
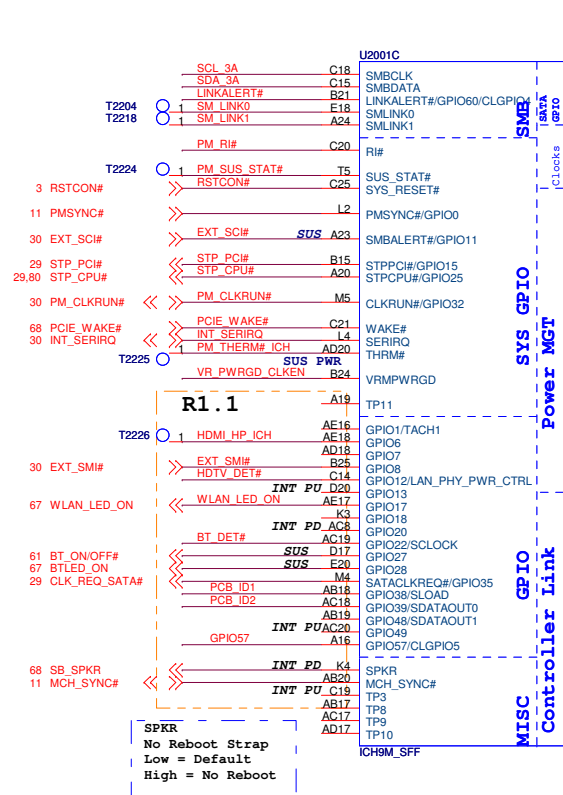
Place within 500 mils of ICH

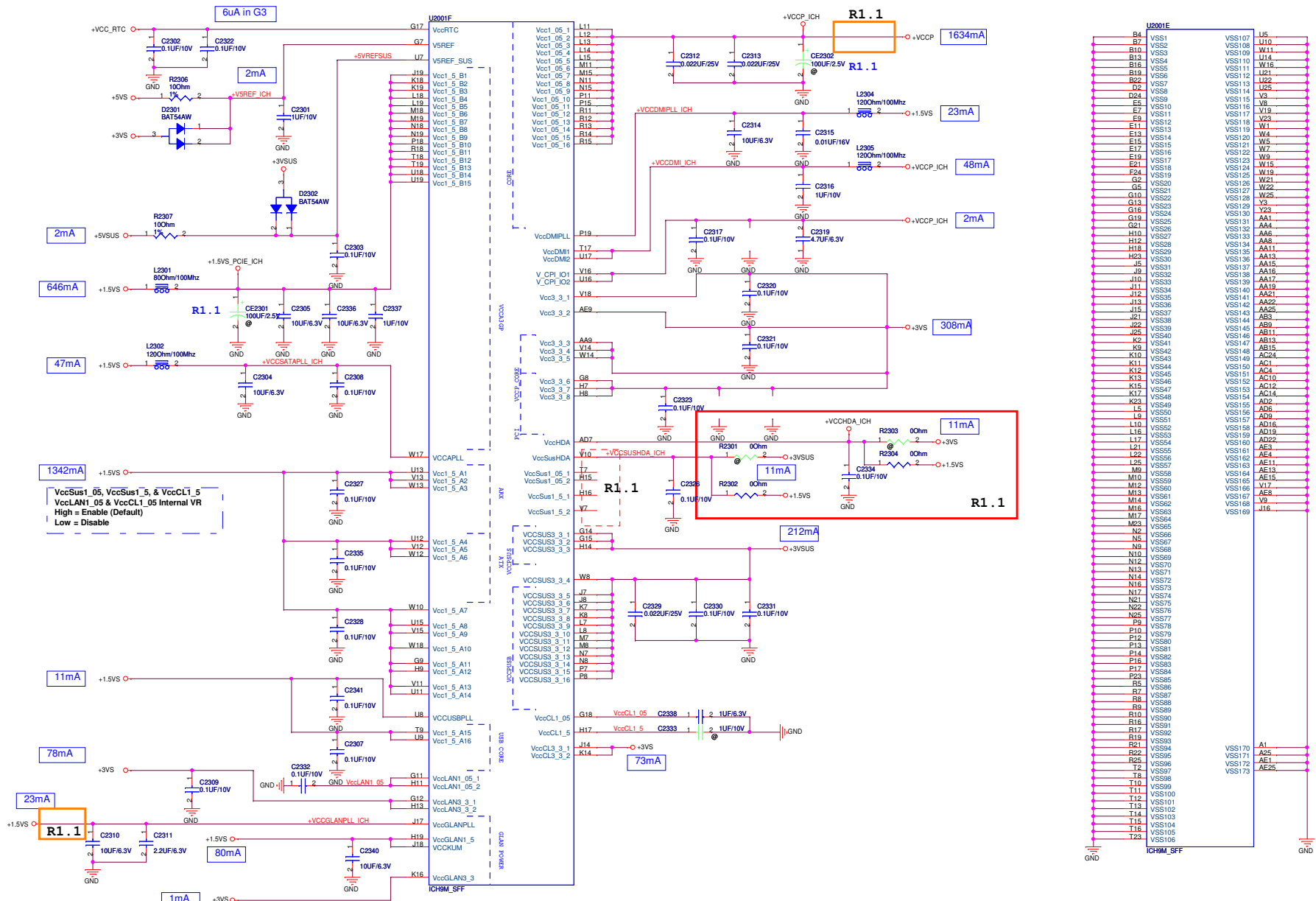


ICH9 Boot BIOS select

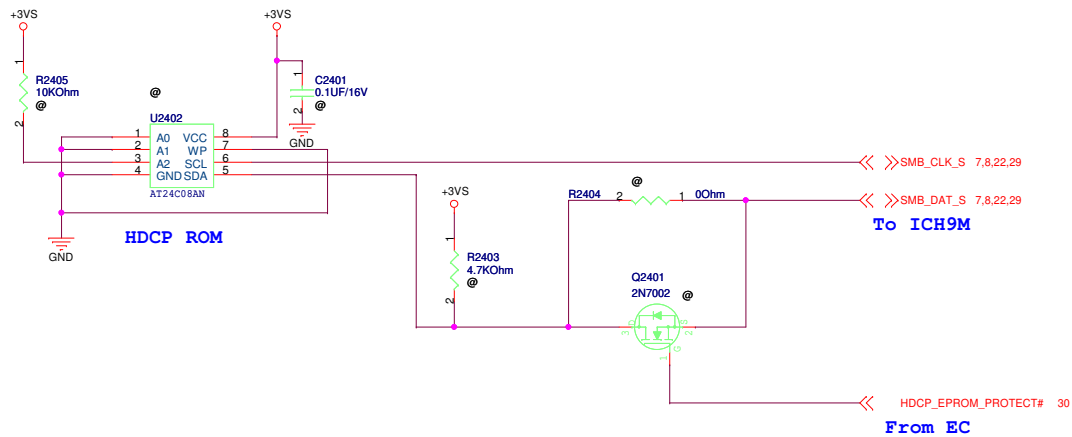
	GNT#0	SPICS#1	
LPC	11	1	(default)
PCI	10	0	
SPI	01	1	

- USB 0 USB Conn.
- USB 1 USB Conn.
- USB 2 Bluetooth
- USB 3
- USB 4 CMOS Camera
- USB 5 Card Reader
- USB 6 WiMax
- USB 7
- USB 8
- USB 9
- USB 10 USB Conn.
- USB 11





U2001E	Pin	Signal	Current
B4	VSS1		
B7	VSS107		
B10	VSS108		
B13	VSS109		
B16	VSS110		
B19	VSS111		
B22	VSS112		
D2	VSS113		
D24	VSS114		
E7	VSS115		
E9	VSS116		
E11	VSS117		
E13	VSS118		
E14	VSS119		
E17	VSS120		
F21	VSS121		
F24	VSS122		
G2	VSS123		
G5	VSS124		
G10	VSS125		
G13	VSS126		
G16	VSS127		
G19	VSS128		
G21	VSS129		
H10	VSS130		
H12	VSS131		
H18	VSS132		
H23	VSS133		
J6	VSS134		
J9	VSS135		
J11	VSS136		
J14	VSS137		
J15	VSS138		
J21	VSS139		
J22	VSS140		
J25	VSS141		
K0	VSS142		
K10	VSS143		
K11	VSS144		
K12	VSS145		
K13	VSS146		
K16	VSS147		
K17	VSS148		
K23	VSS149		
L5	VSS150		
L9	VSS151		
L10	VSS152		
L16	VSS153		
L17	VSS154		
L21	VSS155		
L22	VSS156		
L26	VSS157		
M9	VSS158		
M10	VSS159		
M12	VSS160		
M14	VSS161		
M15	VSS162		
M16	VSS163		
M17	VSS164		
M23	VSS165		
N2	VSS166		
N6	VSS167		
N9	VSS168		
N10	VSS169		
N12	VSS170		
N13	VSS171		
N14	VSS172		
N16	VSS173		
N17	VSS174		
N21	VSS175		
N22	VSS176		
N25	VSS177		
P9	VSS178		
P10	VSS179		
P12	VSS180		
P14	VSS181		
P16	VSS182		
P20	VSS183		
R6	VSS184		
R7	VSS185		
R8	VSS186		
R9	VSS187		
R10	VSS188		
R16	VSS189		
R17	VSS190		
R19	VSS191		
R21	VSS192		
R22	VSS193		
R25	VSS194		
T2	VSS195		
T8	VSS196		
T10	VSS197		
T11	VSS198		
T12	VSS199		
T13	VSS200		
T14	VSS201		
T15	VSS202		
T16	VSS203		
T23	VSS204		
	VSS205		
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	VSS368		
	VSS369		
	VSS370		
	VSS371		
	VSS372		
	VSS373		



<Variant Name>

ASUS		Title : SB ICH9M (5)	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	UL50AT	2.0	
Date: Friday, October 16, 2009	Sheet 24 of 97		

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<Variant Name>

		Title :
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu
Size	Project Name	Rev
C	UL50AT	2.0
Date: Friday, October 16, 2009		Sheet 26 of 97

5

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<Variant Name>

		Title :
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu
Size	Project Name	Rev
C	UL50AT	2.0
Date: Friday, October 16, 2009		Sheet 26 of 97

5

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<Variant Name>

		Title :
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu
Size	Project Name	Rev
C	UL50AT	2.0
Date: Friday, October 16, 2009		Sheet 27 of 97

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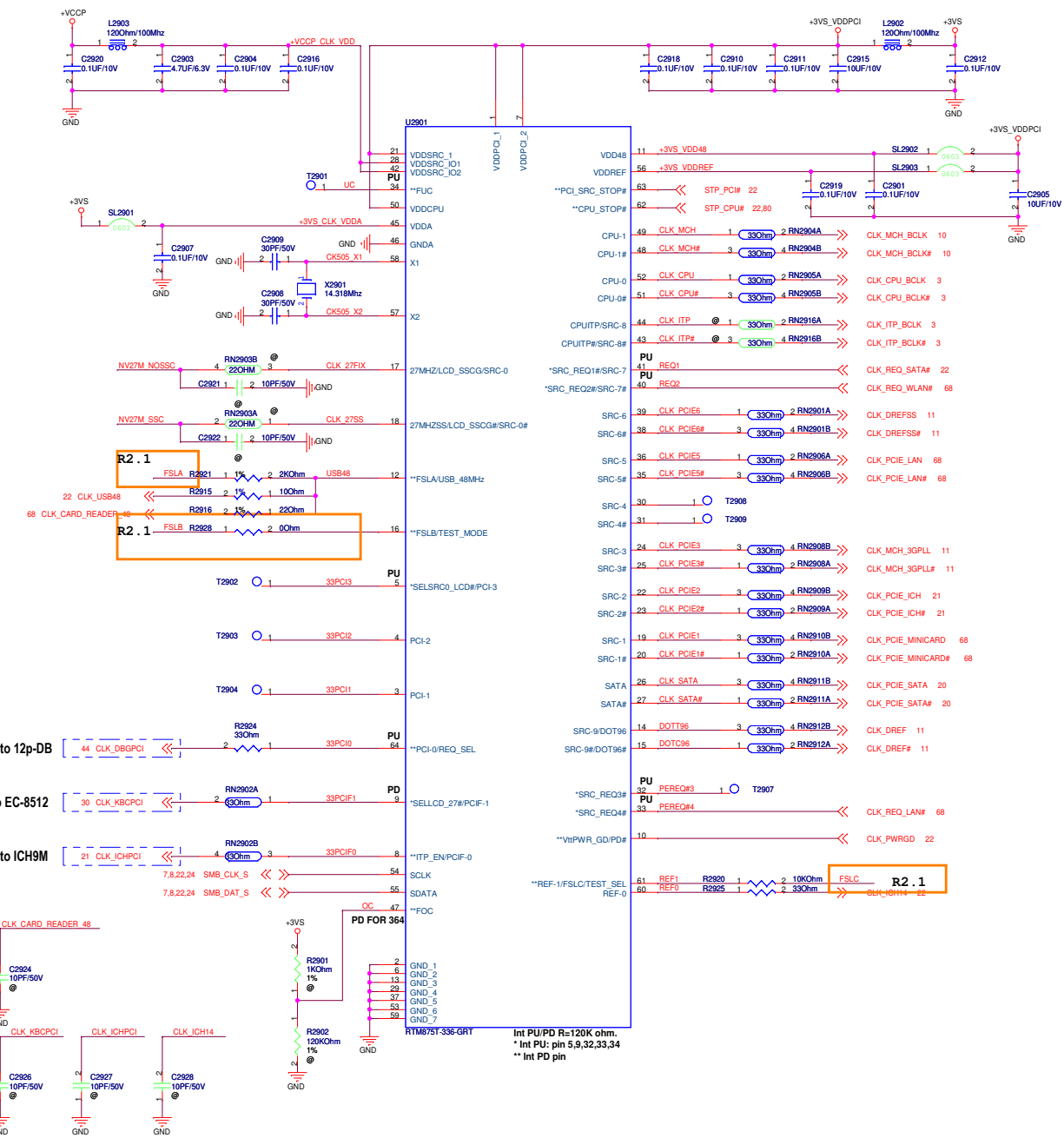
B

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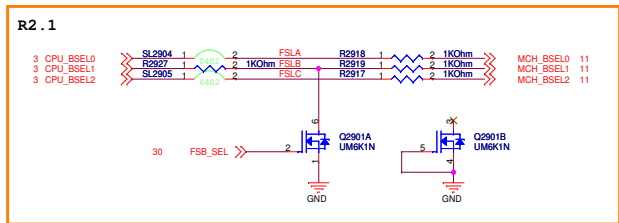
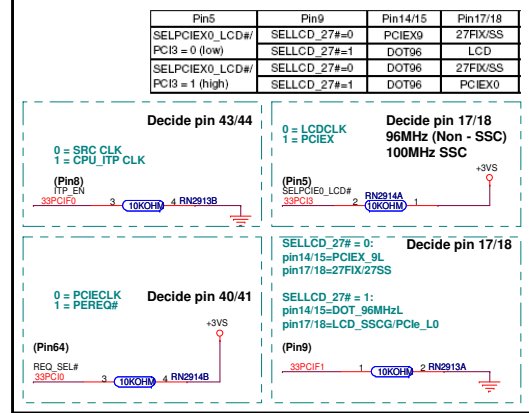
A

<Variant Name>

		Title :
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu
Size	Project Name	Rev
C	UL50AT	2.0
Date: Friday, October 16, 2009		Sheet 28 of 97



Latched Input Select



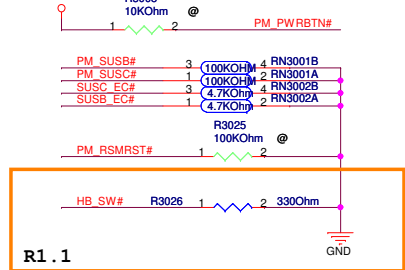
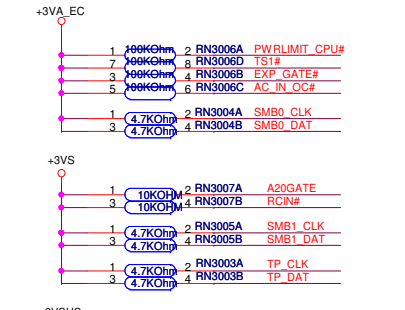
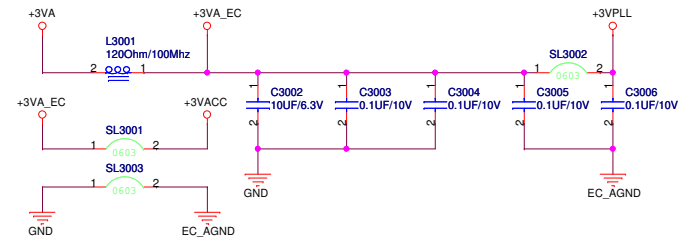
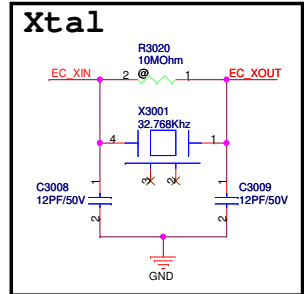
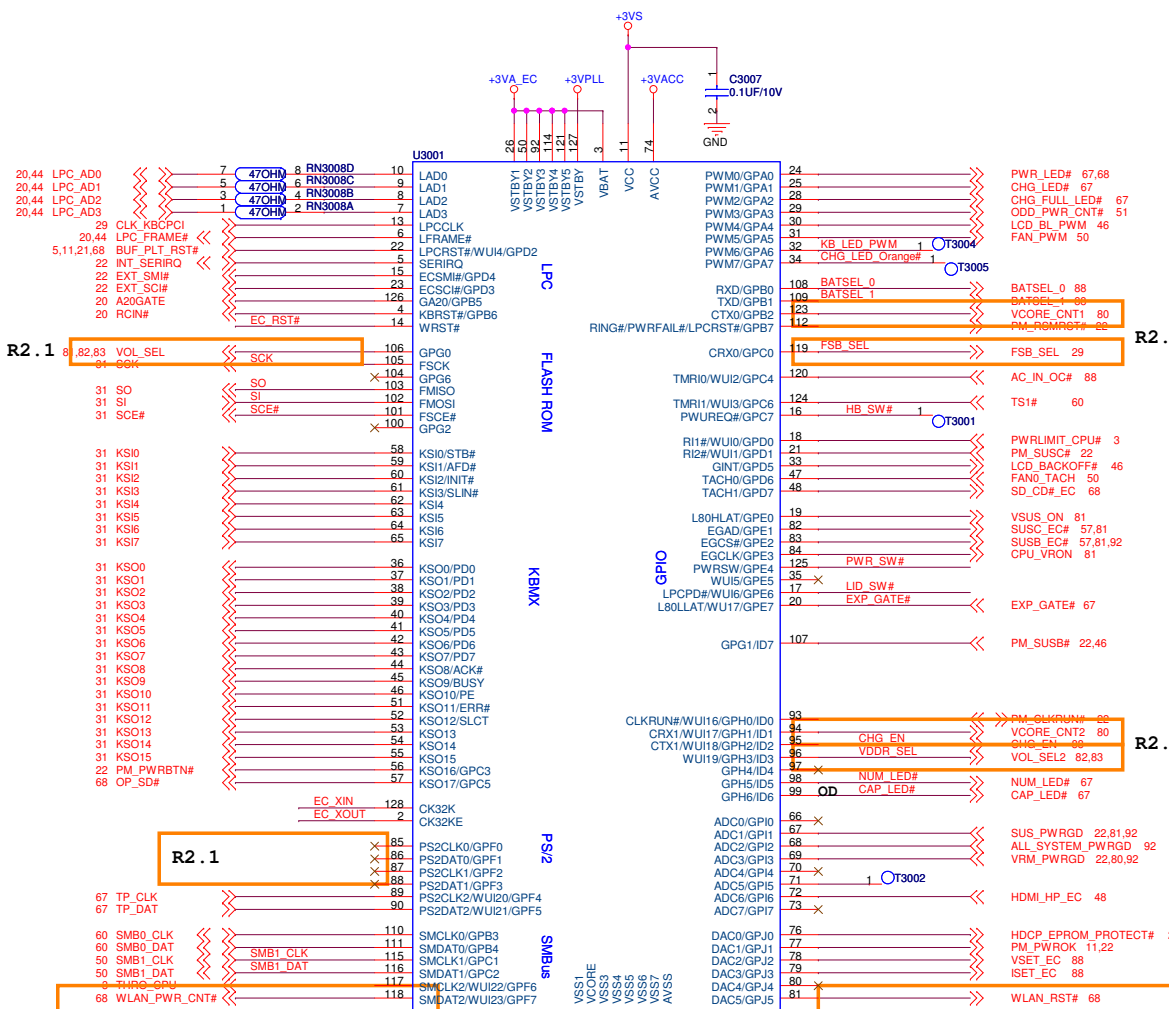
	FSLB	FSLB	FSLA
BCLK	FSB	BSEL2	BSEL1
166	667	0	1
200	800	0	1
266	1066	0	0

to 12p-DB

to EC-8512

to ICH9M

Int PU/PD R=120K ohm.
* Int PU: pin 5,9,32,33,34
** Int PD pin

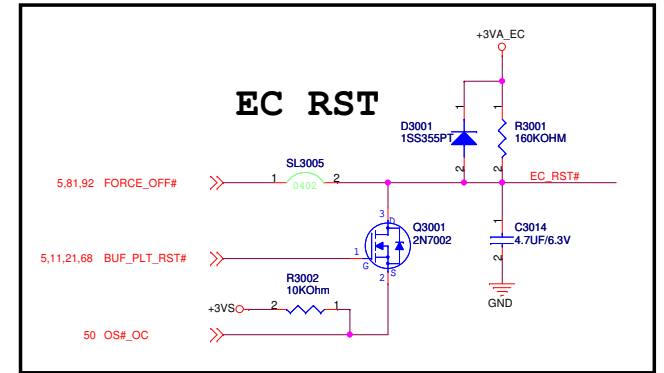
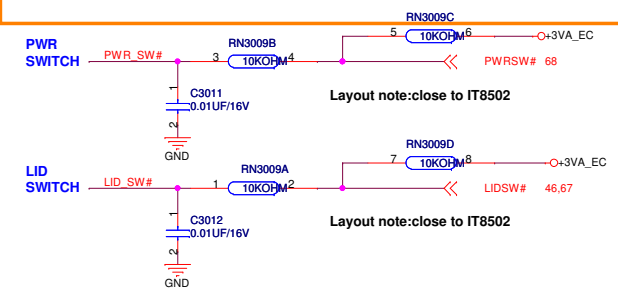


R1.1

R2.1

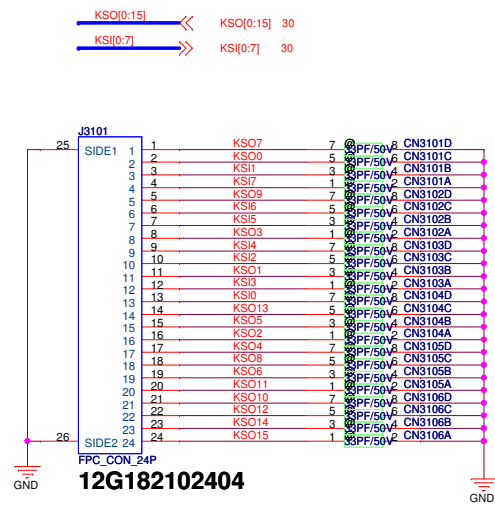
R1.1

R2.1

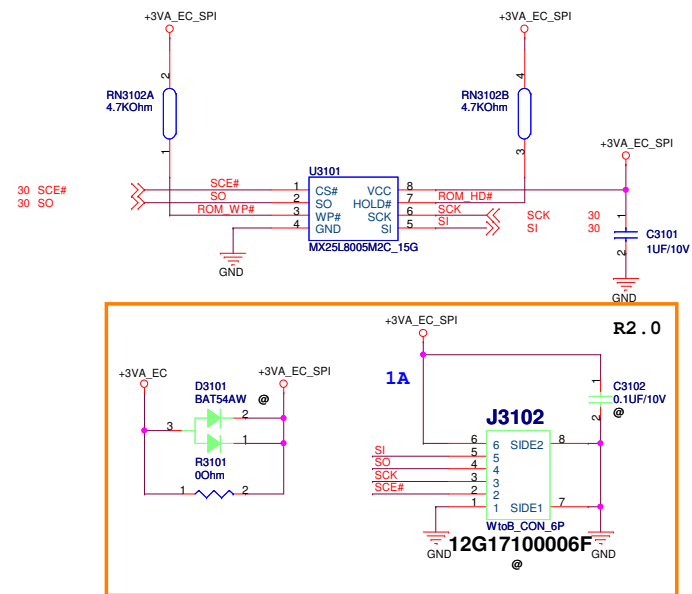


<Variant Name>

Internal Keyboard



SPI Flash ROM (8Mb)



<Variant Name>

ASUS		Title : KB & SPI ROM	
ASUSTek COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
Custom	UL50AT	2.0	
Date: Friday, October 16, 2009	Sheet	31	of 97

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<Variant Name>

		Title: <i>Title</i>	
ASUSTeK COMPUTER INC.		Engineer: <i>Jack Hsu</i>	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: <i>Friday, October 16, 2009</i>		Sheet	32 of 97

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<Variant Name>

		Title : <Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	33 of 97

5

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<Variant Name>

		Title :<Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	34 of 97

5

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<Variant Name>

		Title :<Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	35 of 97

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<Variant Name>

		Title :<Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	38 of 97

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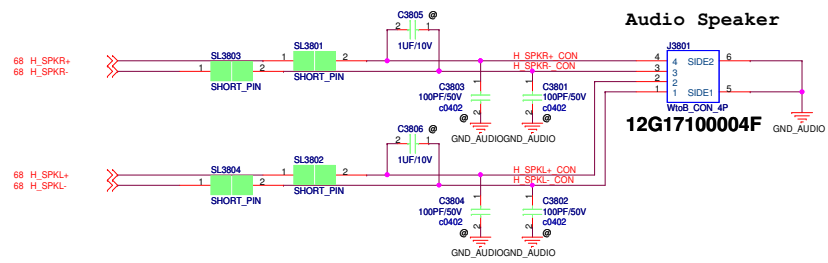
B

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<Variant Name>

		Title :<Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	37 of 97



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<Variant Name>

		Title :<Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	39 of 97

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<Variant Name>

		Title :
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu
Size	Project Name	Rev
C	UL50AT	2.0
Date: <u>Friday, October 16, 2009</u>		Sheet 40 of 97

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<Variant Name>

		Title :
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu
Size	Project Name	Rev
C	UL50AT	2.0
Date: Friday, October 16, 2009		Sheet 41 of 97

5

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<Variant Name>

		Title :<Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	42 of 97

5

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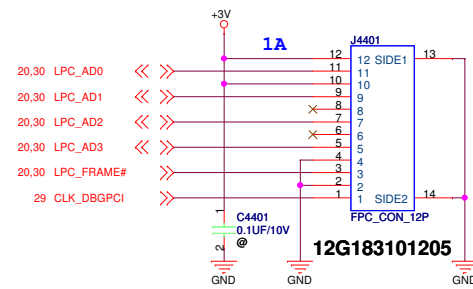
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A

<Variant Name>

		Title :<Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	43 of 97

LPC DEBUG PORT



<Variant Name>

ASUS		Title : DEBUG PORT	
ASUSTeK COMPUTER INC.		Engineer: <i>Jack Hsu</i>	
Size	Project Name	Rev	
Custom	UL50AT	2.0	
Date: Friday, October 16, 2009	Sheet	44	of 97

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C

C


B

B

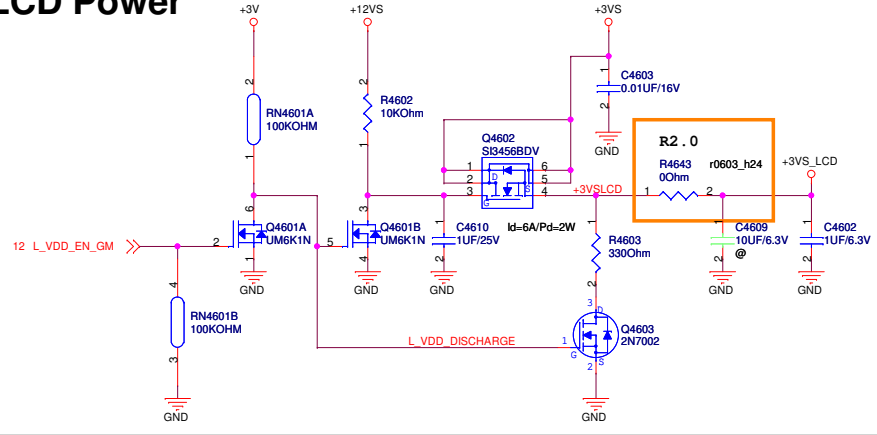
A

A

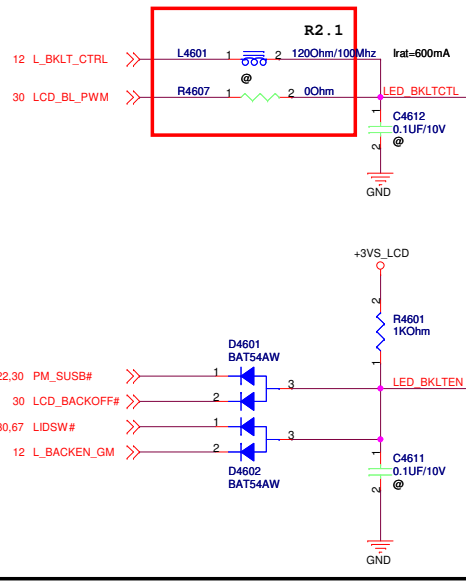
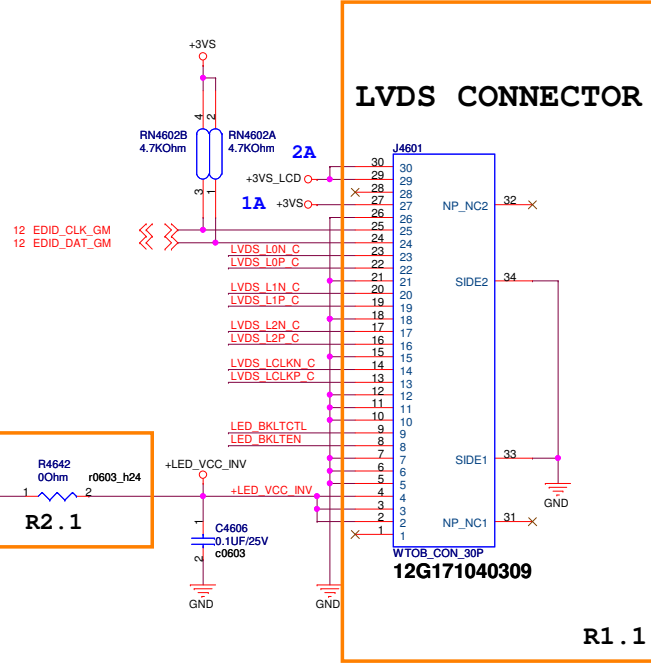
<Variant Name>

		Title :<Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	45 of 97

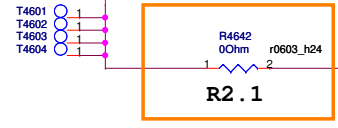
LCD Power



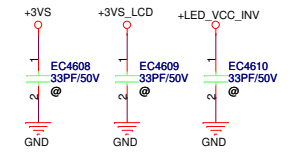
LVDS CONNECTOR



AC_BAT_SYS



- 12 LVDS_L0N_GM >>> 1 SLN4601A LVDS_L0N_C
- 12 LVDS_L0P_GM >>> 3 SLN4601B LVDS_L0P_C
- 12 LVDS_L1N_GM >>> 1 SLN4602A LVDS_L1N_C
- 12 LVDS_L1P_GM >>> 3 SLN4602B LVDS_L1P_C
- 12 LVDS_L2N_GM >>> 1 SLN4603A LVDS_L2N_C
- 12 LVDS_L2P_GM >>> 3 SLN4603B LVDS_L2P_C
- 12 LVDS_LCLKN_GM >>> 1 SLN4604A LVDS_LCLKN_C
- 12 LVDS_LCLKP_GM >>> 3 SLN4604B LVDS_LCLKP_C



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<Variant Name>

		Title :<Title>
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu
Size	Project Name	Rev
C	UL50AT	2.0
Date: <u>Friday, October 16, 2009</u>		Sheet 47 of 97



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C

C


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<Variant Name>

		Title : HDMI LEVEL SHIFT
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu
Size C	Project Name UL50AT	Rev 2.0
Date: Friday, October 16, 2009		Sheet 49 of 97

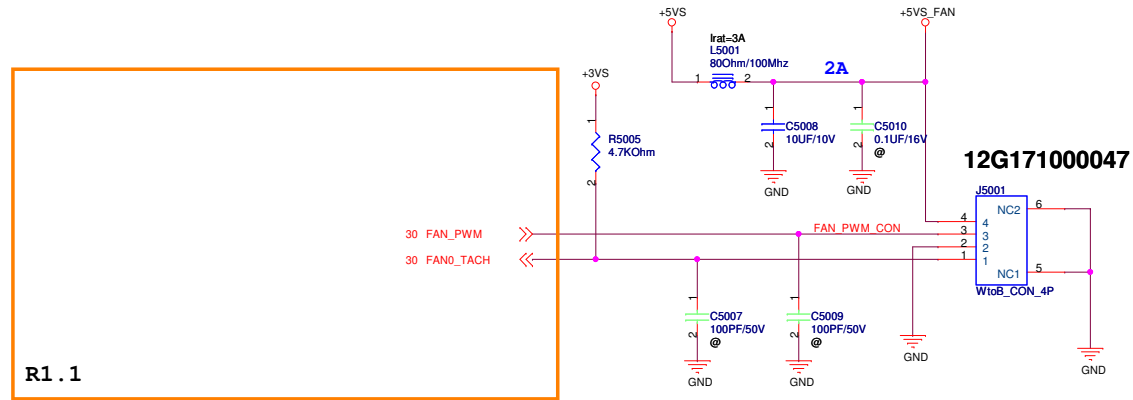
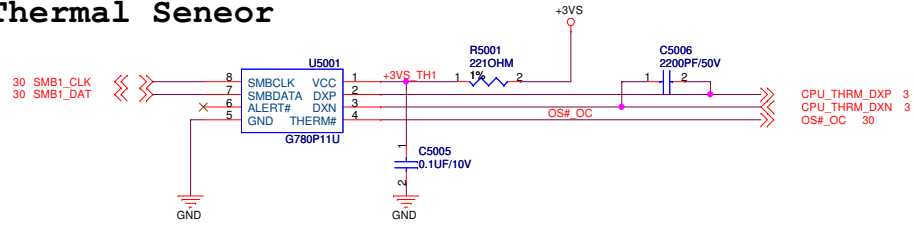
1nd: 06G023096010 G780P11U SOP-8
 2nd: 06G023026012 MAX6657YMS+ SOP-8

Route CPU_THRM_DA , CPU_THRM_DC and MEM_THERM_DA , MEM_THERM_DC on the same layer

-----OTHER SIGNALS
 10 mils
 =====GND
 10 mils
 =====H_THERMDA(10 mils)
 10 mils
 =====H_THERMDC(10 mils)
 10 mils
 =====GND
 10 mils
 -----OTHER SIGNALS

Avoid FSB,Power

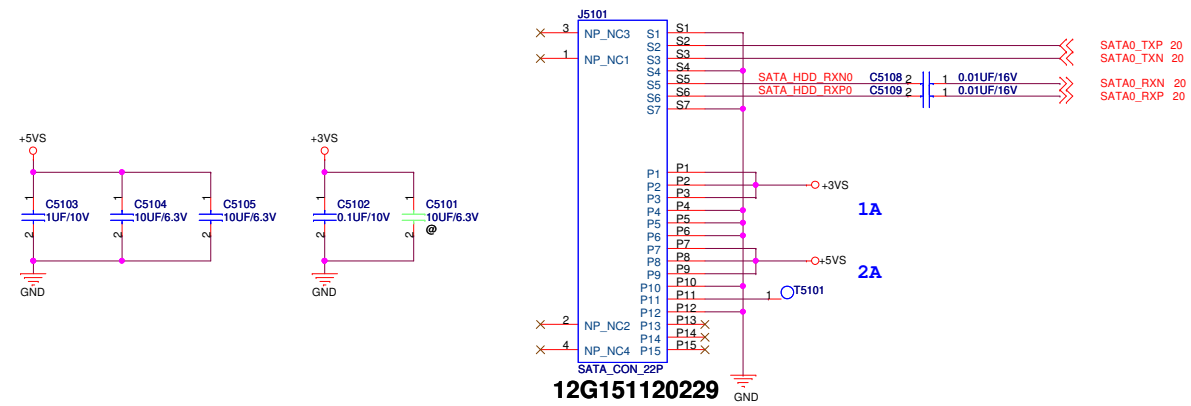
Thermal Seneor



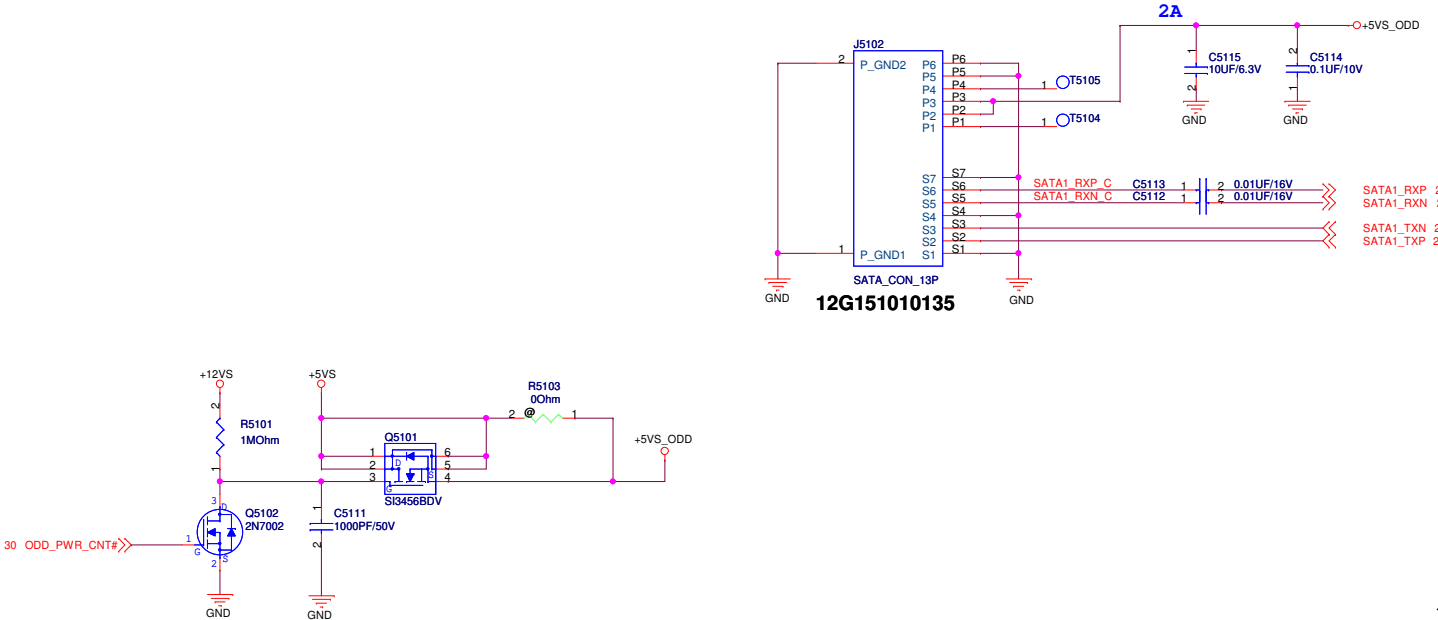
R1.1

<Variant Name>

SATA HDD



SATA ODD



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<Variant Name>

		Title : <Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	52 of 97

5

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<Variant Name>

		Title : <Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	53 of 97

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<Variant Name>

		Title : <Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	54 of 97

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<Variant Name>

		Title : <Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	55 of 97

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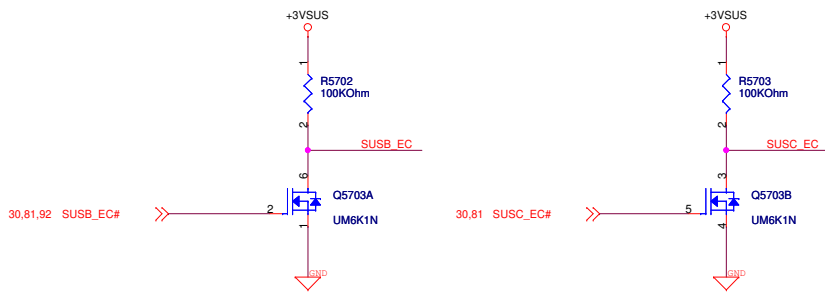
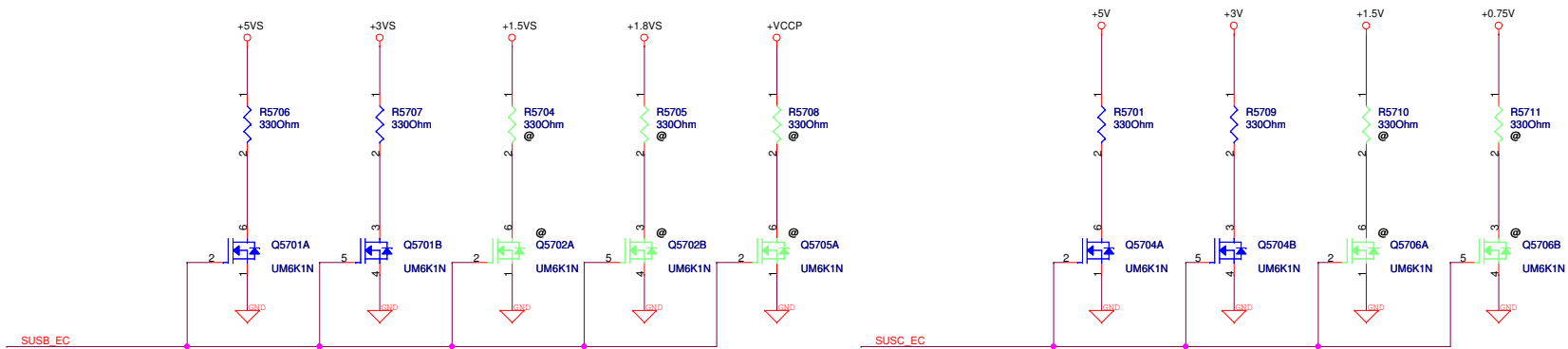
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A

<Variant Name>

		Title : LID	
ASUSTeK COMPUTER INC.		Engineer: <i>Jack Hsu</i>	
Size	Project Name	Rev	
Custom	UL50AT	2.0	
Date:	Friday, October 16, 2009	Sheet	56 of 97

Discharge Circuit



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<Variant Name>

		Title : <Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	56 of 97

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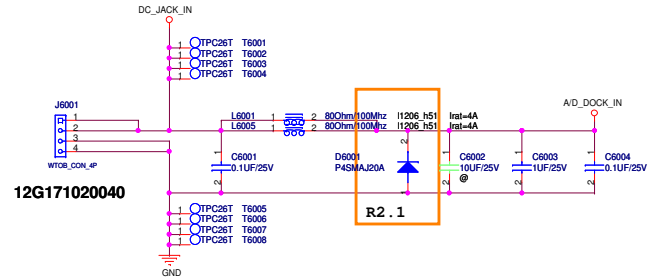
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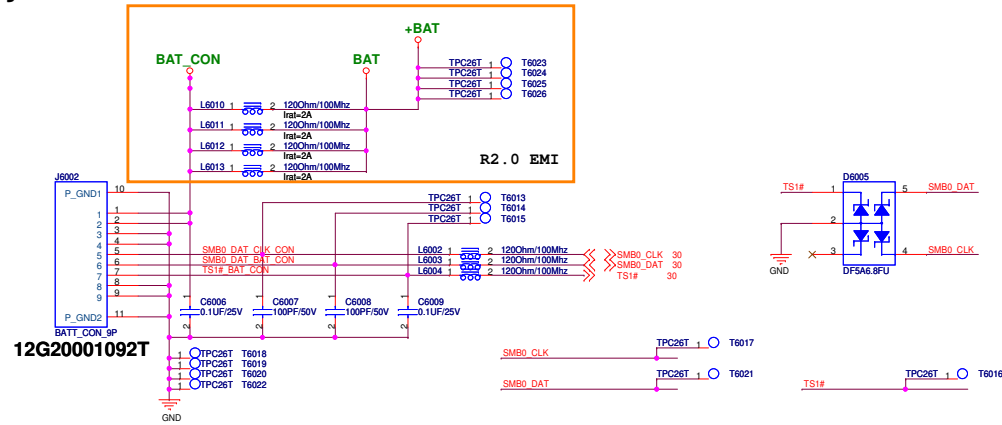
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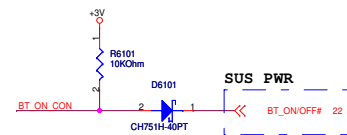
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ASUSTeK COMPUTER INC.		Engineer: Jack Hsu
Size	Project Name	Rev
C	UL50AT	2.0
Date: <u>Friday, October 16, 2009</u>		Sheet 59 of 97

DC-IN



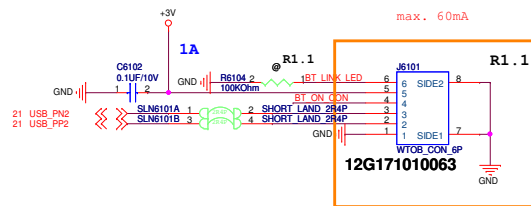
Battery Connector





Bluetooth Connector

max. 60mA



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<Variant Name>

		Title : <Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	62 of 97

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<Variant Name>

		Title : <Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	63 of 97

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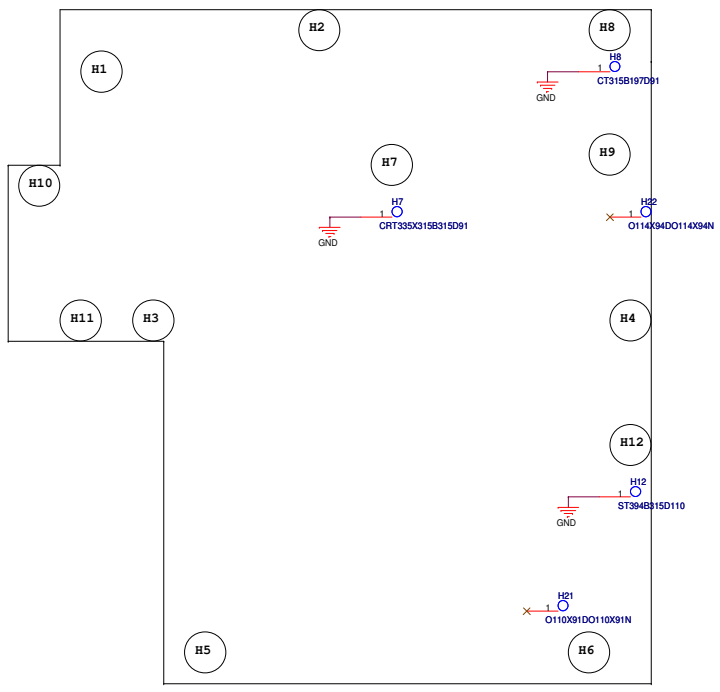
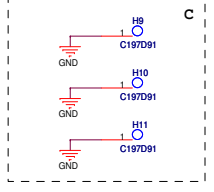
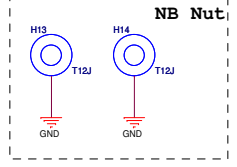
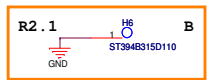
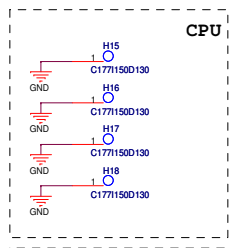
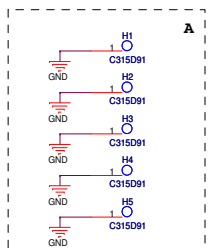
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<Variant Name>

		Title : <Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	64 of 97

Screw Hole & SMT Nut



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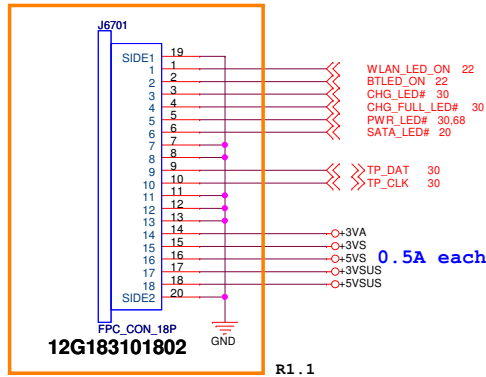
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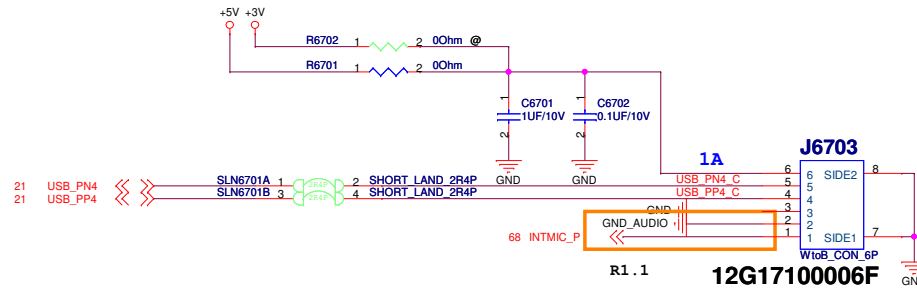
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		Title :
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu
Size	Project Name	Rev
C	UL50AT	2.0
Date: <u>Friday, October 16, 2009</u>		Sheet 66 of 97

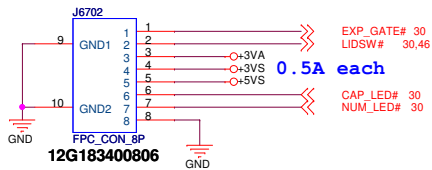
Touch Pad / LED Board



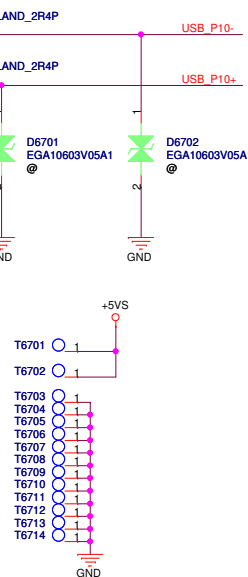
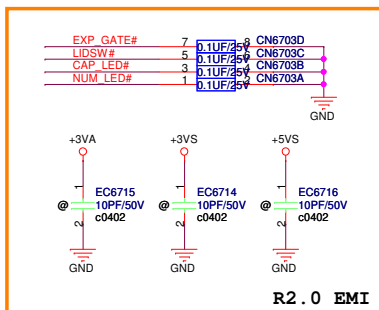
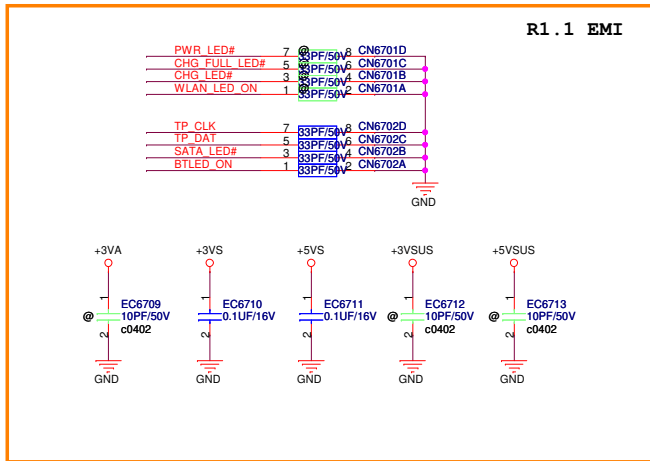
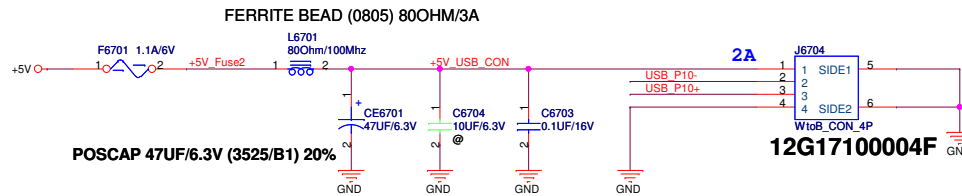
Camera Module



Function Board

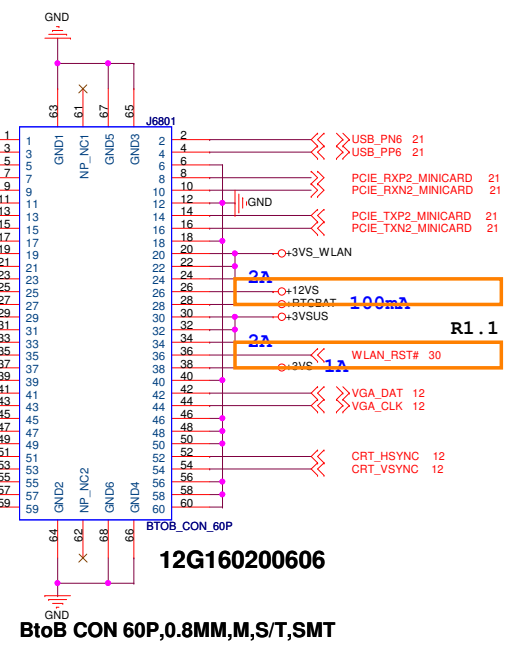
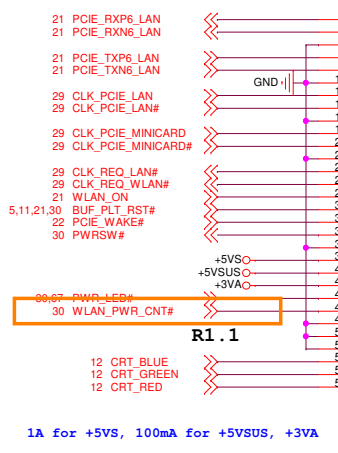
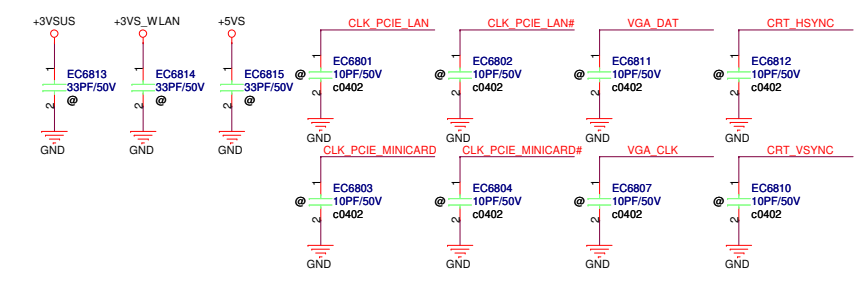
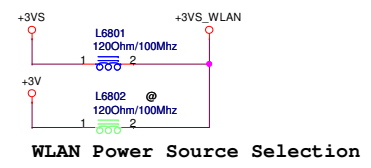


FLY USB Cable



IO BOARD - 02

- LAN IC
- RJ45
- CRT
- RTC Conn.
- MiniCard

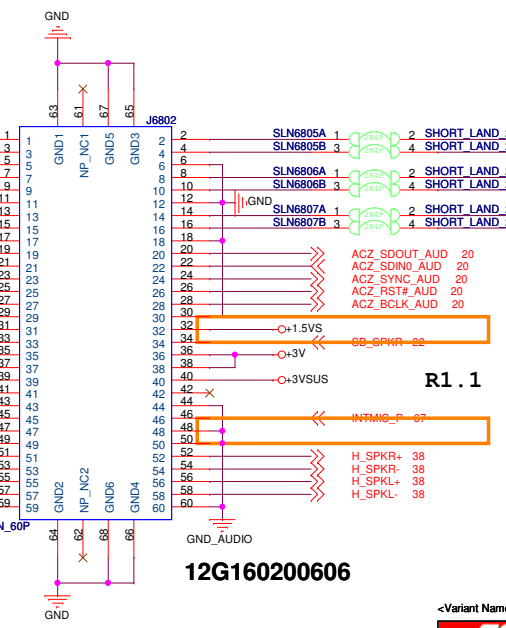
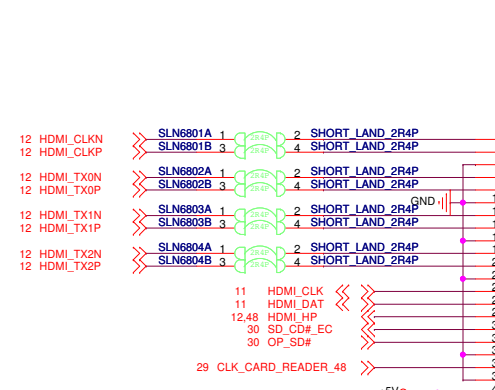
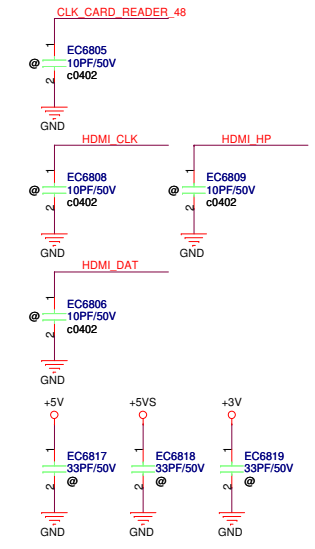


USB 0	USB Conn.
USB 1	USB Conn.
USB 2	Bluetooth
USB 3	
USB 4	CMOS Camera
USB 5	Card Reader
USB 6	WiMax
USB 7	
USB 8	
USB 9	
USB 10	USB Conn.
USB 11	

12G160200606
BtoB CON 60P,0.8MM,M,S/T,SMT

IO BOARD - 01

- HDMI Conn.
- USB Conn. x2
- MIC-IN Conn.
- Head Phone Conn.
- Audio IC
- Card Reader IC
- Card Reader Conn.



USB_PN5	21
USB_PP5	21
USB_PN0	21
USB_PP0	21
USB_PN1	21
USB_PP1	21

12G160200606
BtoB CON 60P,0.8MM,M,S/T,SMT

ASUS Title : **B TO B CONNECTOR**
 ASUSTek COMPUTER INC. Engineer: **Jack Hsu**
 Size Project Name
 Custom **UL50AT** Rev 2.0
 Date: Friday, October 16, 2009 Sheet 68 of 97

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<Variant Name>

		Title : <Title>	
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	69 of 97

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		Title: M10M-GE1 (1)	
ASUSTeK COMPUTER INC.		Engineer: Alan Chen	
Size C	Project Name UL50AT	Rev 2.0	Date Friday, October 16, 2009
Sheet 70 of 97			

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		Title: M10M-GE1 (2)	
ASUSTeK COMPUTER INC.		Engineer: Alan Chen	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	71 of 97

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		Title: M10M-GE1 (3)	
<small>ASUSTeK Corporation</small>		Engineer: Alan Chen	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	72 of 97

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		Title: M10M-GE1 (4)	
ASUSTeK COMPUTER INC.		Engineer: Alan Chen	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	78 of 97

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		Title: M10M-GE1 (5)	
ASUSTeK COMPUTER INC.		Engineer: Alan Chen	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	74 of 97

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		Title: M10M-GE1 (6)
ASUSTeK COMPUTER INC.		Engineer: Alan Chen
Size	Project Name	Rev
C	UL50AT	2.0
Date: Friday, October 16, 2009		Sheet 78 of 97

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		Title VGA Power Sequence	
ASUSTeK COMPUTER INC.		Engineer: Alan Chen	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	76 of 97

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		Title: <Title>	
ASUSTeK COMPUTER INC.		Engineer: Alan Chen	
Size	Project Name	Rev	
C	UL50AT <Variant Name>	2.0	
Date: Friday, October 16, 2009		Sheet	77 of 97

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		Title:	
ASUSTeK COMPUTER INC.		Engineer: Alan Chen	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	78 of 97

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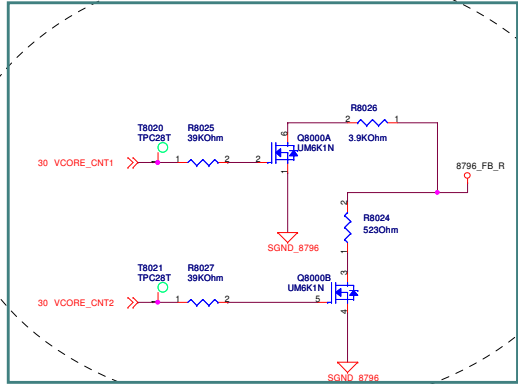
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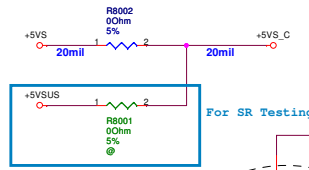
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ASUSTeK COMPUTER INC.		Engineer: Alan Chen	
Size	Project Name	Rev	
C	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	79 of 97

R2.1 7/29 for OC

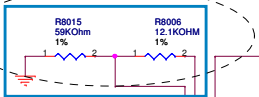


CPU VID=1.2V

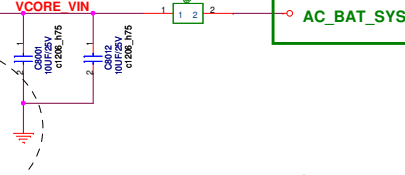
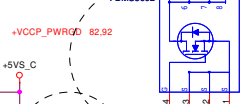
VCORE_CNT1	VCORE_CNT2	Voltage	Offset
H	H	1.3988V	VID+222mV
H	L	1.3488V	VID+26mV
L	H	1.25V	VID+196mV
L	L	1.2V	VID



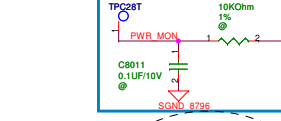
modify 10/15 for OC



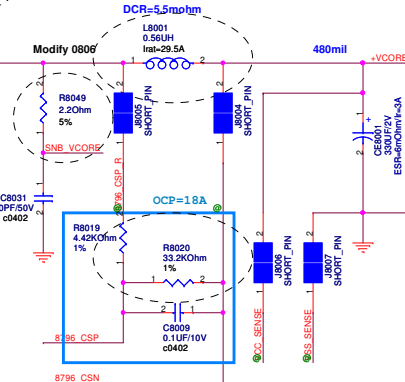
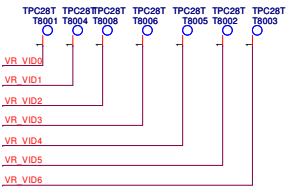
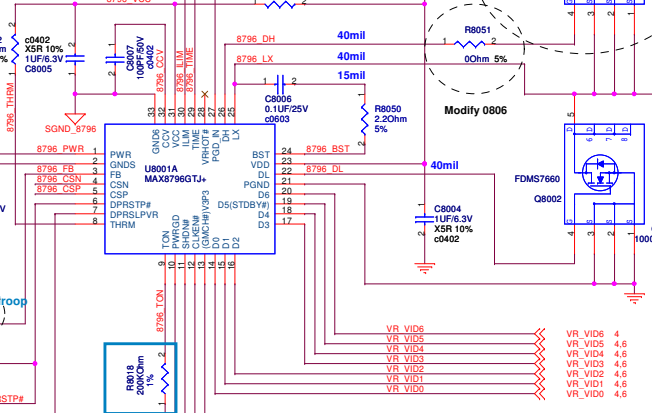
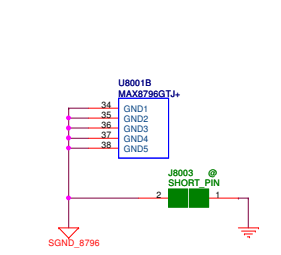
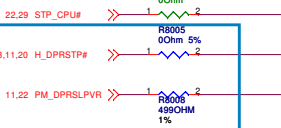
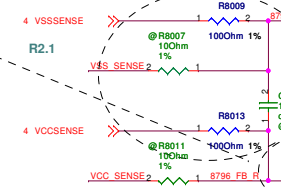
Modify 05/18



Power monitor



modify 10/15 for OC



Total count: 37 pcs

- T8013 TPC28T
- CPU_VRON_PWR 1
- T8014 TPC28T
- CLK_EN# 1
- T8015 TPC28T
- VRM_PWRGD 1
- T8028 TPC28T
- GND 1
- T8029 TPC28T
- GND 1
- T8032 TPC28T
- 1
- T8018 TPC28T
- VSSSENSE 1
- T8019 TPC28T
- +VSUS_C 1
- T8009 TPC28T
- +VCORE 1
- T8030 TPC28T
- GND 1
- T8023 TPC28T
- GND 1
- T8028 TPC28T
- GND 1
- T8029 TPC28T
- GND 1

<Variant Name>

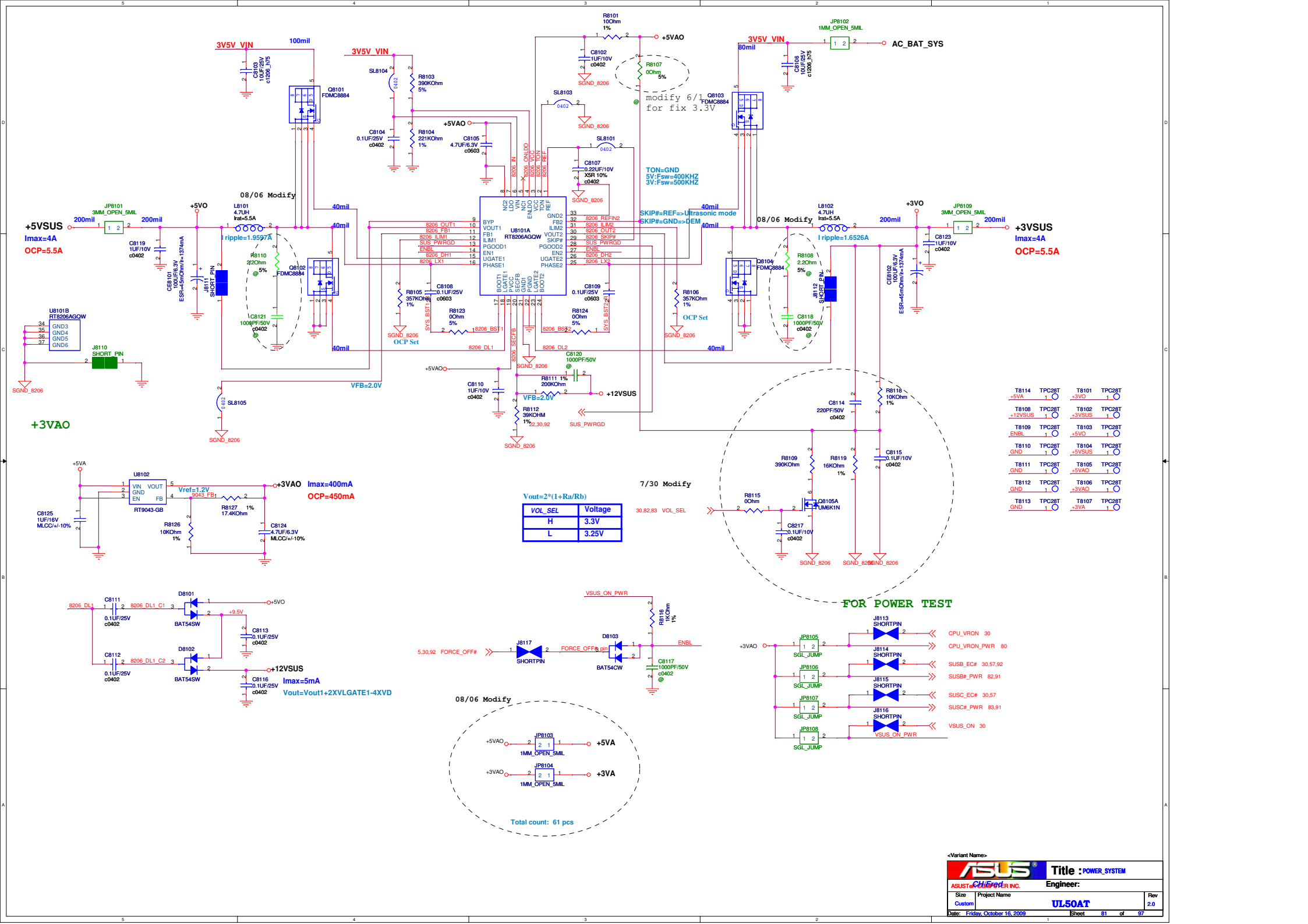


Title : POWER_VCORE

ASUSTek COMPUTER INC. CH/Fre Engineer:

Size Project Name UL50AT Rev 2.0

Custom Date: Friday, October 16, 2009 Sheet 60 of 97



+5VSUS
I_{max}=4A
OCP=5.5A

+3VAO

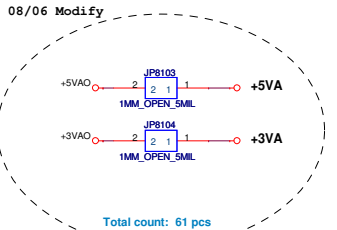
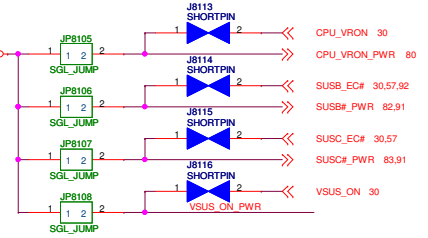
+3VAO I_{max}=400mA
OCP=450mA

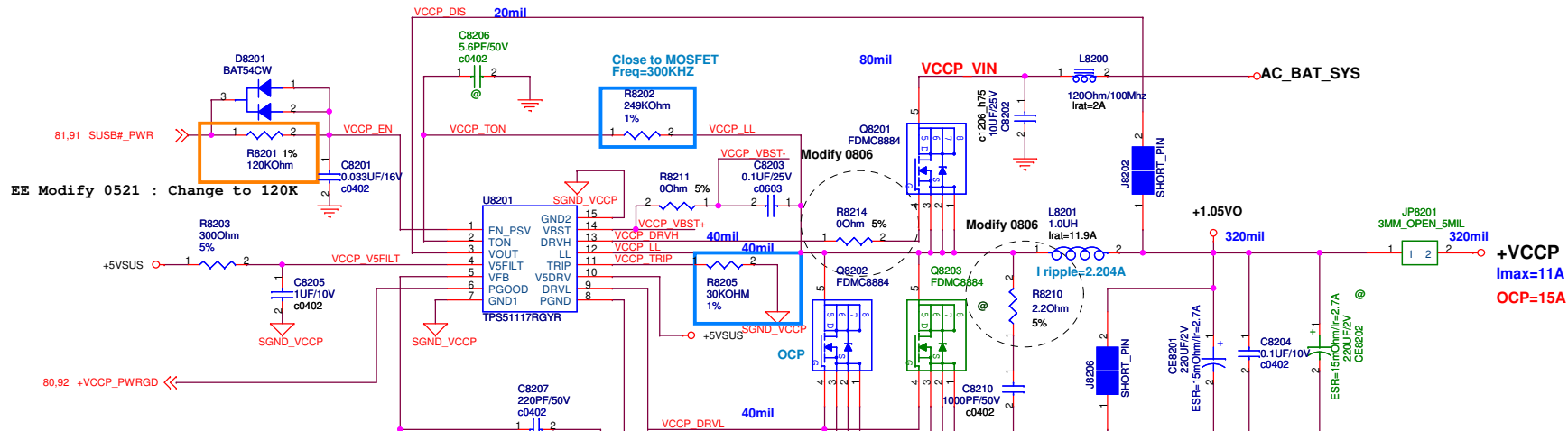
+12VSUS I_{max}=5mA
V_{out}=V_{out1}+2XVLGATE1-4XVD

VOL_SEL	Voltage
H	3.3V
L	3.25V

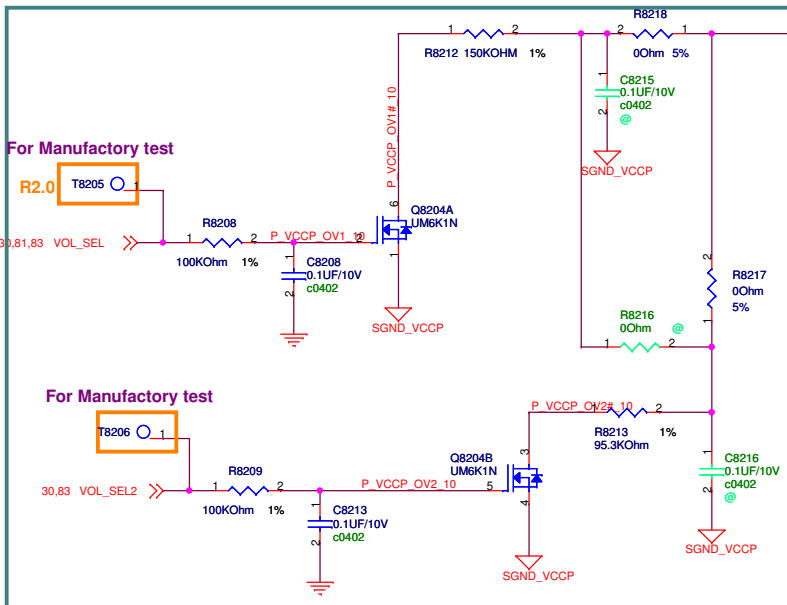
- T8114 TPC28T +5VA
- T8108 TPC28T +12VSUS
- T8109 ENBL
- T8110 TPC28T GND
- T8111 TPC28T GND
- T8112 TPC28T GND
- T8113 TPC28T GND
- T8101 TPC28T +3VO
- T8102 TPC28T +3VSUS
- T8103 TPC28T +5VO
- T8104 TPC28T +5VSUS
- T8105 TPC28T +5VAO
- T8106 TPC28T +3VAO
- T8107 TPC28T +3VA

FOR POWER TEST





R2.1 Modify 7/29 for OC



VOL_SEL2	VOL_SEL	Voltage
L	L	1V
L	H	1.05V
H	L	N/A(1.079V)
H	H	1.129V

- T8201 TPC28T
- +1.05VO 1
- T8202 TPC28T
- +VCCP 1
- T8203 TPC28T
- GND 1
- T8204 TPC28T
- GND 1

Close to IC

Total count: 20 pcs

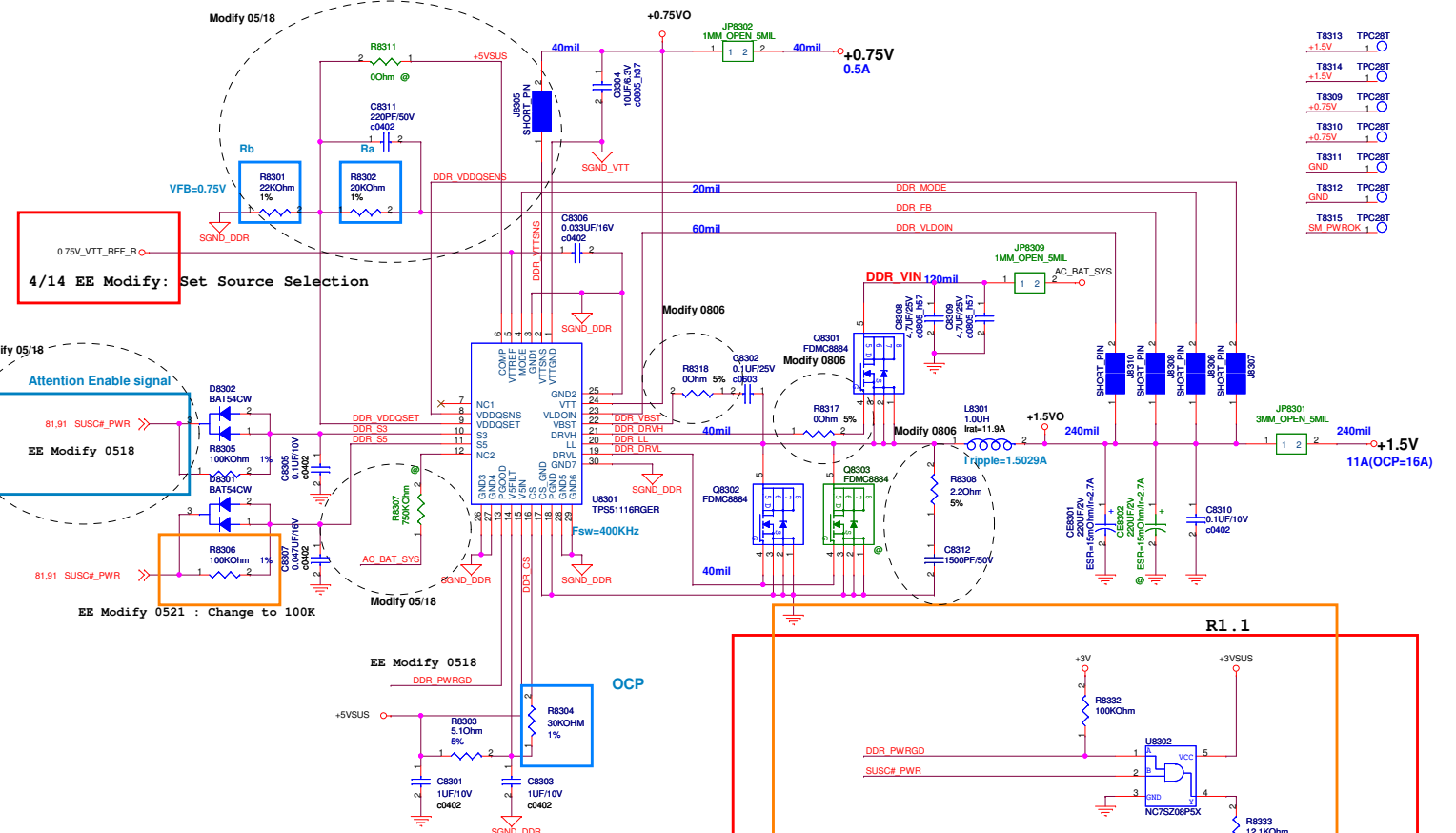
<Variant Name>

ASUS Title : POWER_IO_+VCCP

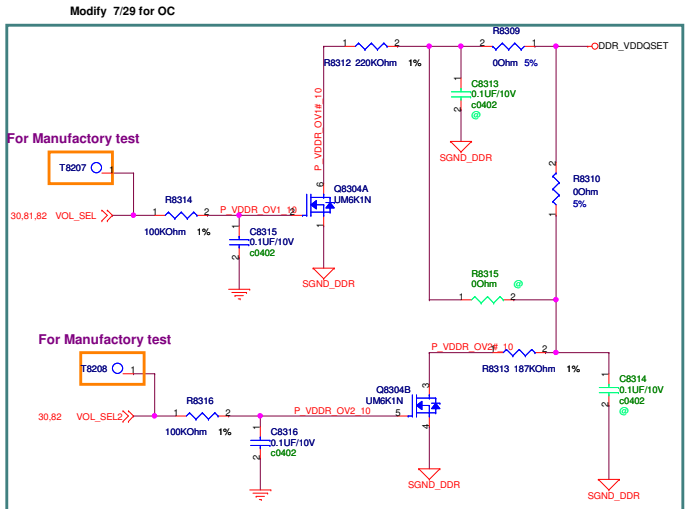
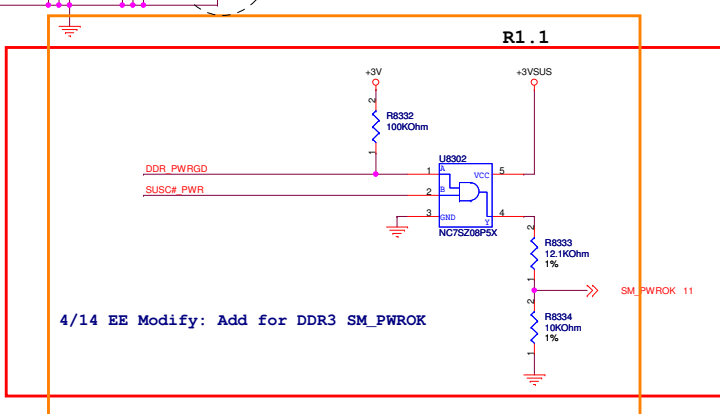
ASUSTek COMPUTER INC. Engineer:

Size	Project Name	Rev
Custom	UL50AT	2.0

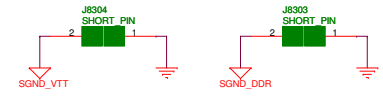
Date: Friday, October 16, 2009 Sheet 82 of 97



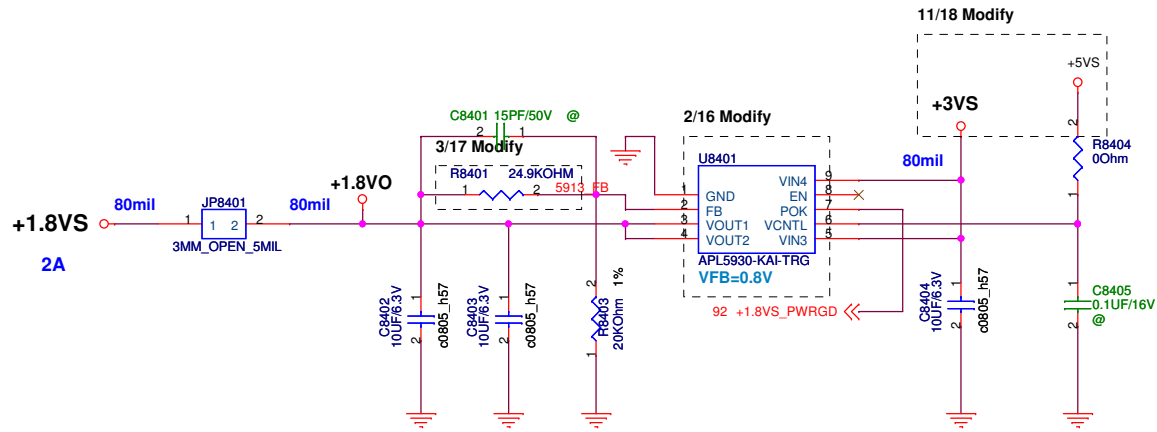
T8313	TPC28T	+1.5V
T8314	TPC28T	+1.5V
T8309	TPC28T	+0.75V
T8310	TPC28T	+0.75V
T8311	TPC28T	GND
T8312	TPC28T	GND
T8315	TPC28T	SM_PWROK



VOL_SEL2	VOL_SEL	Voltage
L	L	1.43V
L	H	1.5V
H	L	N/A(1.512V)
H	H	1.58V



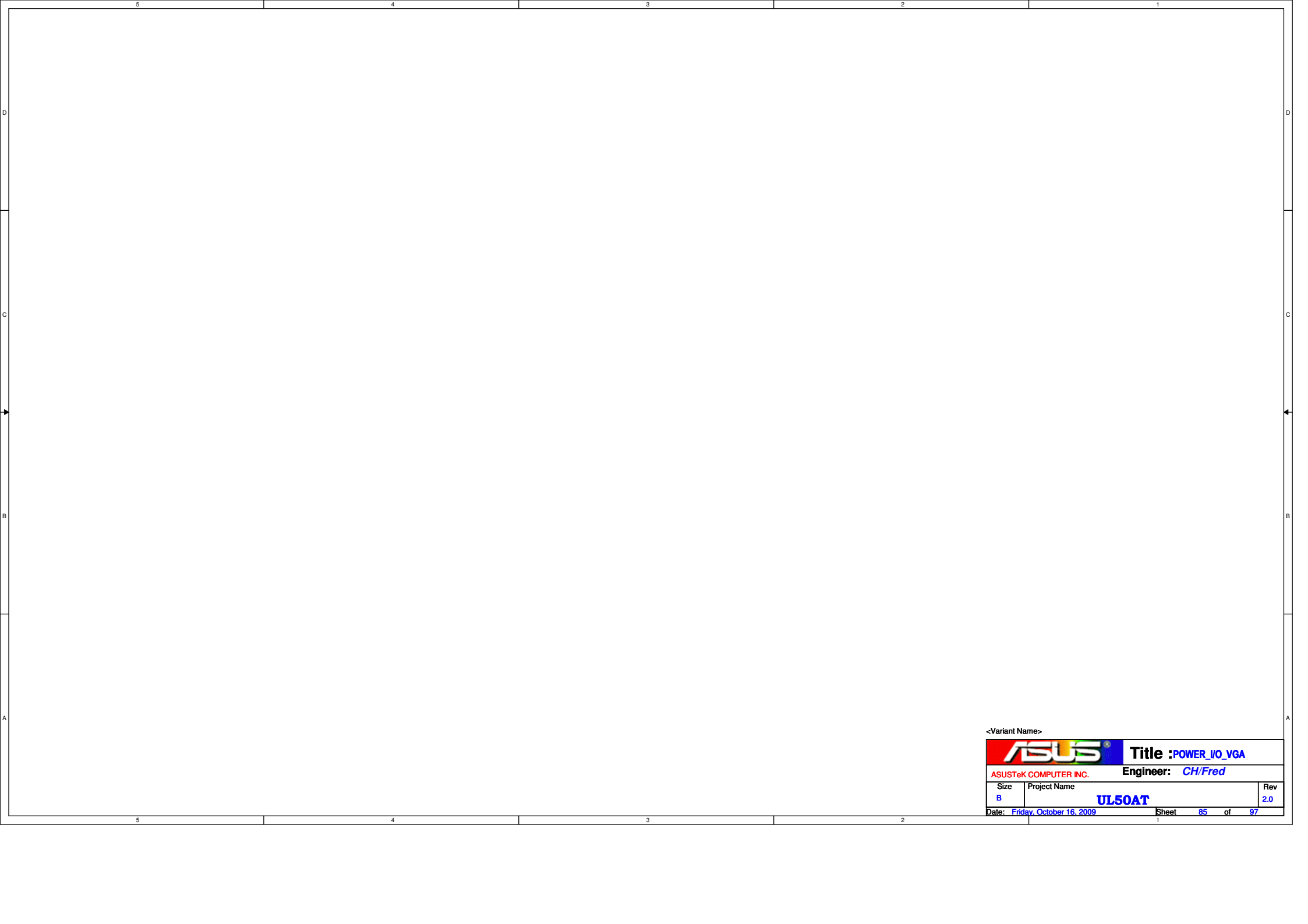
+1.8VS




- T8401 TPC28T
+1.8VO 1
- T8402 TPC28T
+1.8VS 1
- T8403 TPC28T
GND 1
- T8404 TPC28T
GND 1

<Variant Name>

		Title : POWER_IO_+1.8VS	
ASUSTeK COMPUTER INC.		Engineer: CH/Fred	
Size	Project Name		Rev
Custom	UL50AT		2.0
Date: Friday, October 16, 2009		Sheet	84 of 97




<Variant Name>

		Title : POWER_I/O_VGA
ASUSTeK COMPUTER INC.		Engineer: CH/Fred
Size	Project Name	Rev
B	UL50AT	2.0
Date: Friday, October 16, 2009		Sheet 85 of 97



<Variant Name>

		Title : <Title>	
ASUSTeK COMPUTER INC.		Engineer: CH/Fred	
Size	Project Name	Rev	
Custom	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	86 of 97

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<Variant Name>

		Title : <Title>	
ASUSTeK COMPUTER INC.		Engineer: CH/Fred	
Size	Project Name	Rev	
A	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	87 of 97

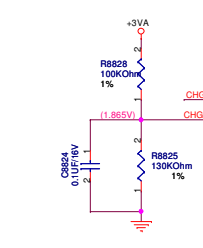
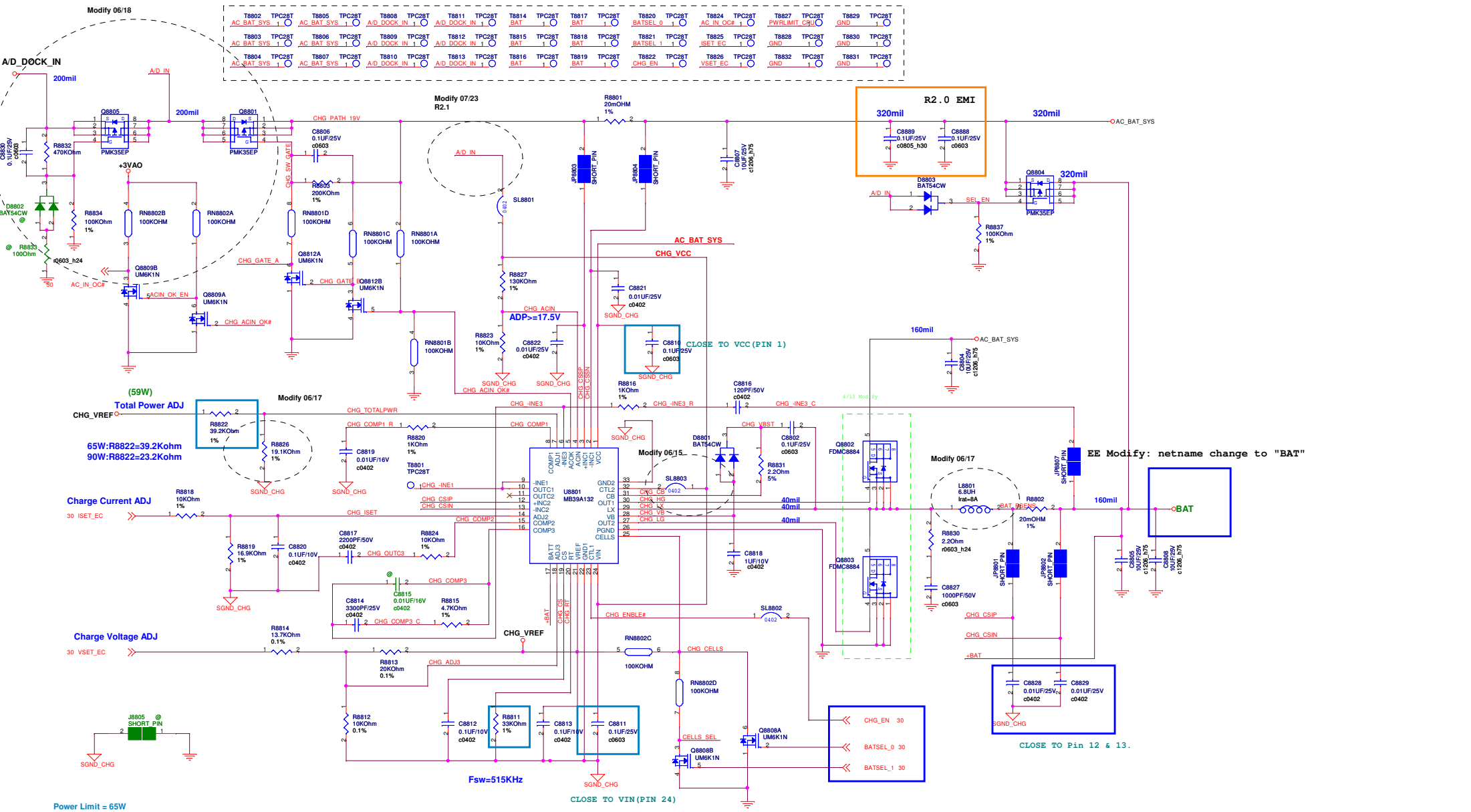
5

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TOTAL COUNT:56 PCS

Battery Cells		
BATSEL_1	BATSEL_0	CELLS
H	H	2 CELLS
L	H	2 CELLS
H	L	3 CELLS
L	L	4 CELLS

Charger IC and EC Code correlation sheet :
 Charger MAX8725 => EC CODE : 200
 Charger MAX17015 => EC CODE : 201
 Charger MB39A132 => EC CODE : 202

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<Variant Name>

		Title : <Title>	
ASUSTeK COMPUTER INC.		Engineer: CH/Fred	
Size	Project Name	Rev	
A	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet	89 of 97

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<Variant Name>

		Title : POWER_DETECT	
ASUSTeK COMPUTER INC.		Engineer: CH/Fred	
Size	Project Name	Rev	
Custom	UL50AT	2.0	
Date: Friday, October 16, 2009		Sheet 90 of 97	

5

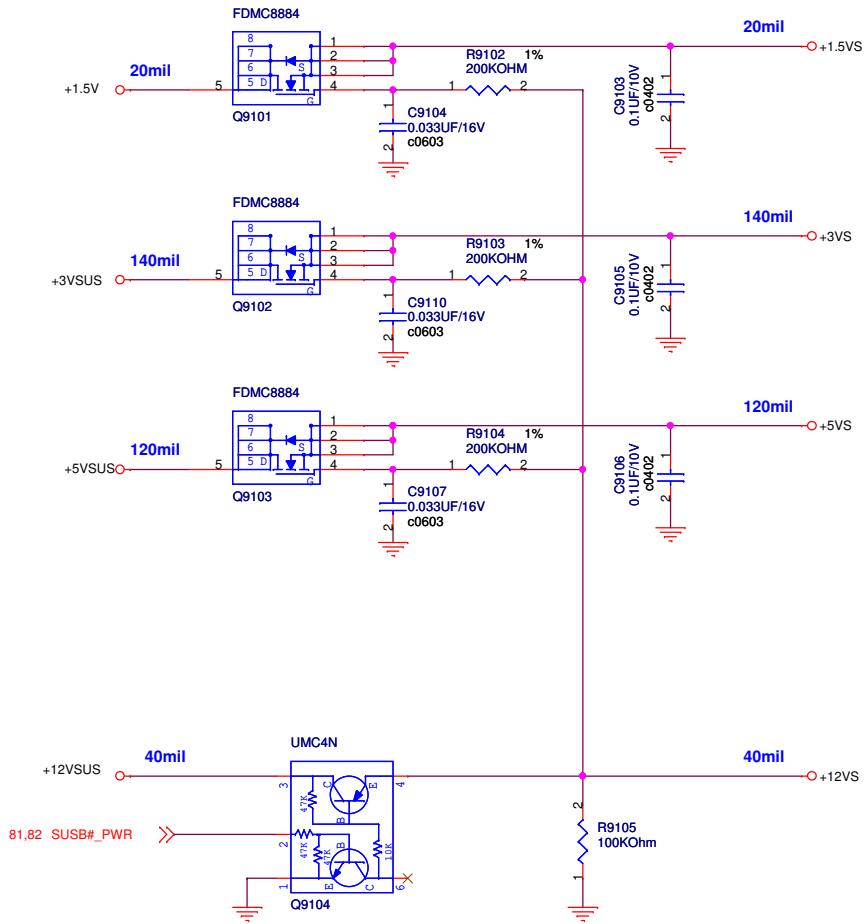
4

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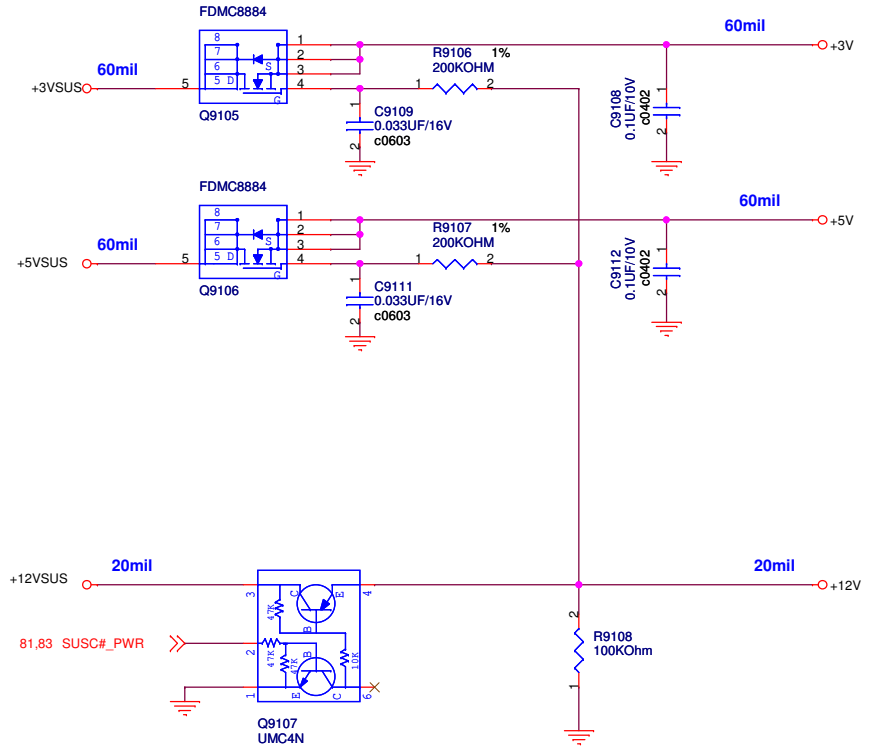
1

SUSB#_PWR POWER



Total count: 19 pcs

SUSC#_PWR POWER

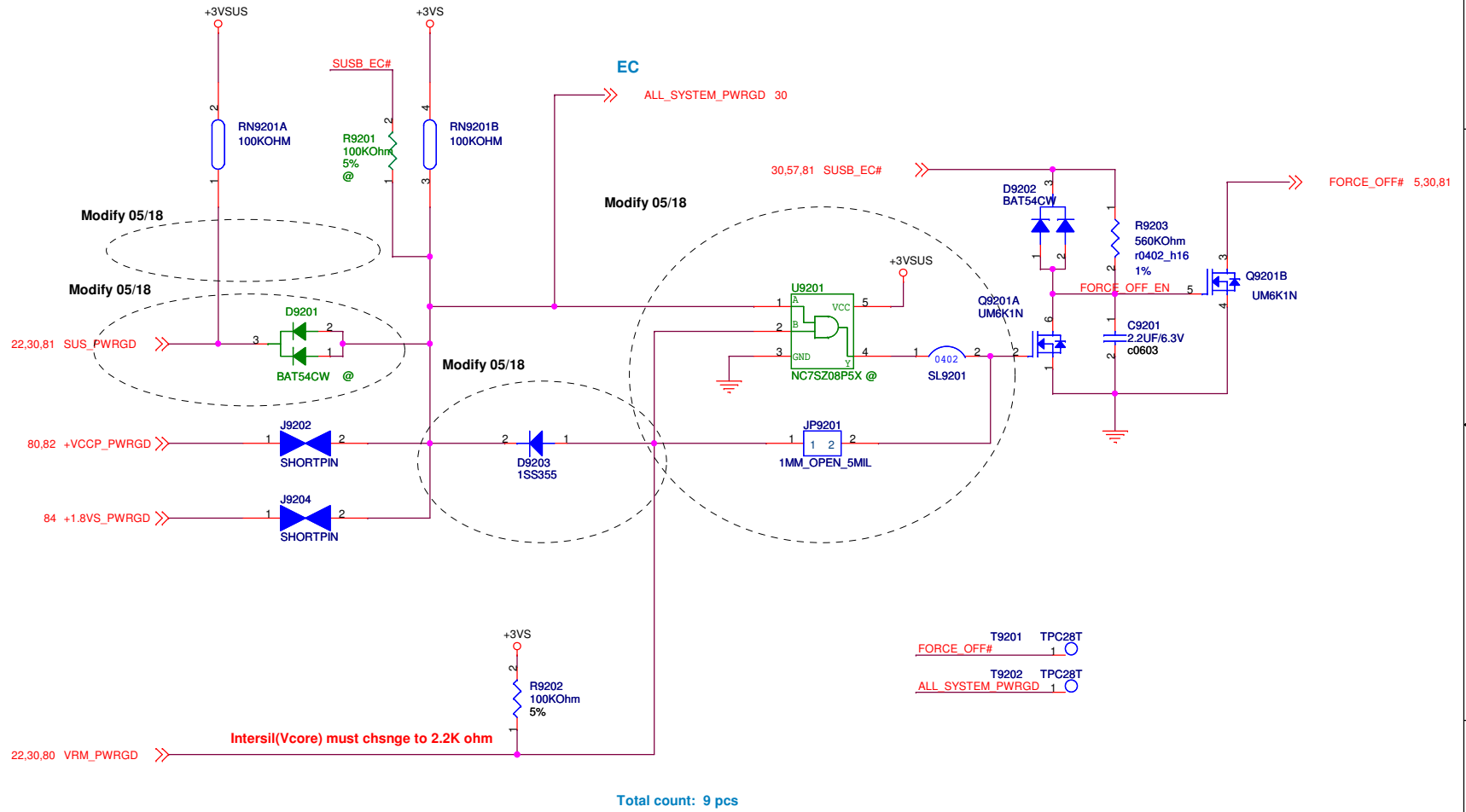


T9101	TPC28T	T9111	TPC28T
+12VSUS	1	+3VSUS	1
T9102	TPC28T	T9113	TPC28T
+12VS	1	+3VS	1
T9103	TPC28T	T9115	TPC28T
+12V	1	+3V	1
T9104	TPC28T	T9120	TPC28T
+5VSUS	1	+1.5V	1
T9106	TPC28T	T9121	TPC28T
+5V	1	+1.5VS	1
T9110	TPC28T	T9123	TPC28T
+5V	1	SUSB#_PWR1	1
		T9114	TPC28T
		SUSC#_PWR1	1

<Variant Name>

ASUS		Title :POWER_LOAD SWITCH	
ASUSTeK COMPUTER INC.		Engineer: CH/Fred	
Size	Project Name	Rev	
B	UL50AT	2.0	
Date: Friday, October 16, 2009	Sheet	91	of 97

POWER GOOD DETECTOR



<Variant Name>		ASUS		Title :POWER_PROTECT	
ASUSTeK COMPUTER INC.		Engineer:		CH/Fred	
Size	Project Name			Rev	
B	UL50AT			2.0	
Date: Friday, October 16, 2009		Sheet		92	of 97

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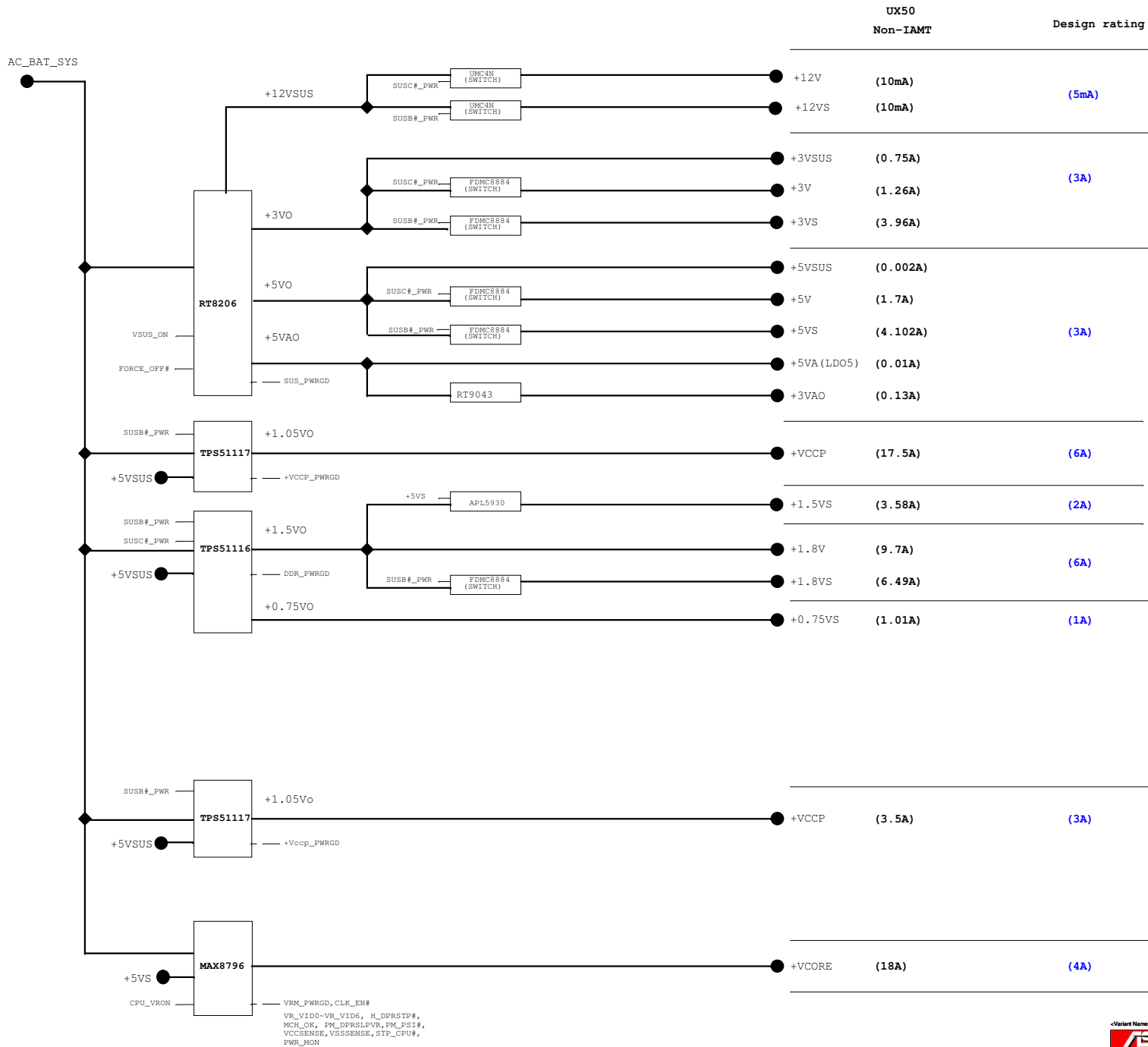
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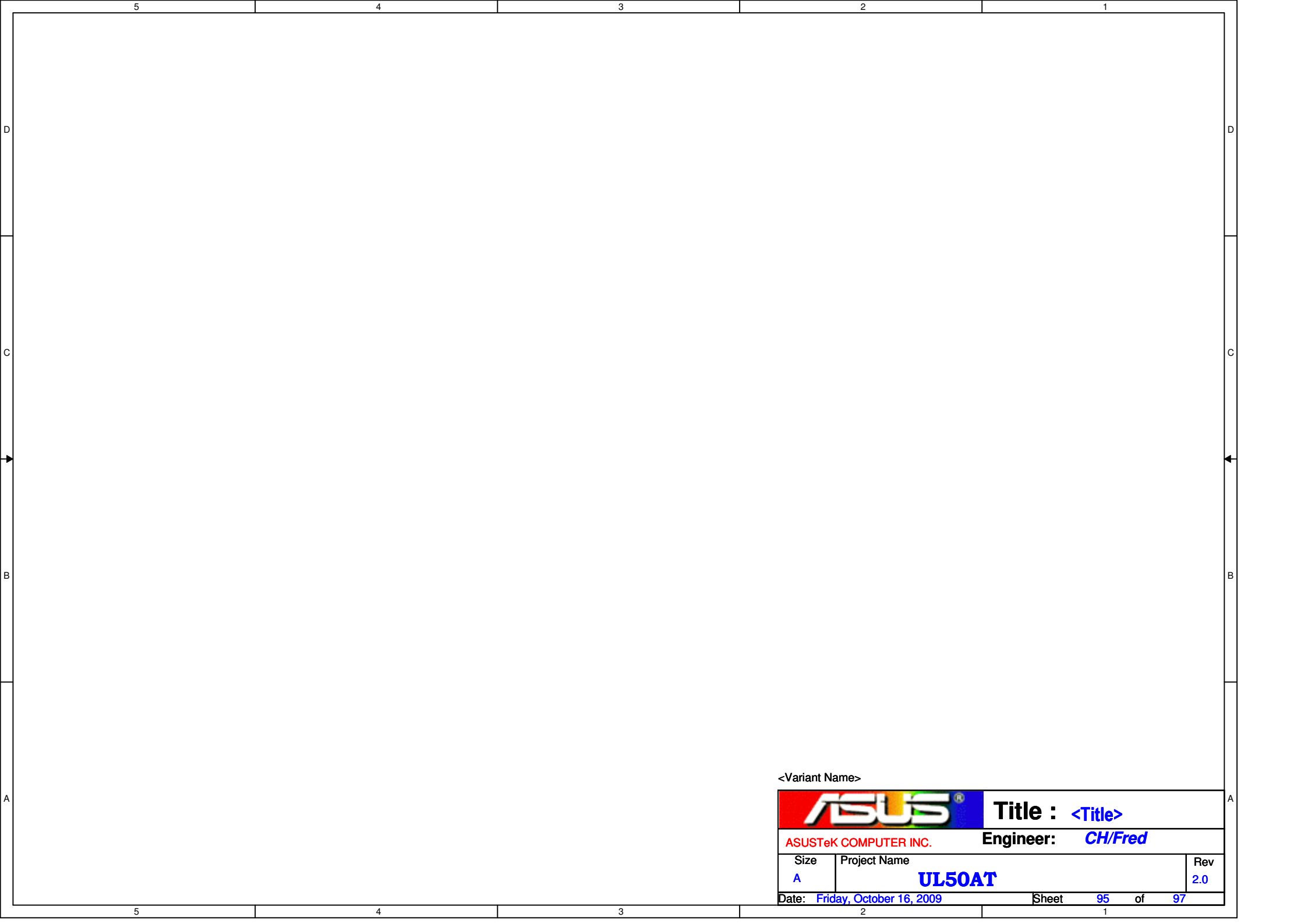
A

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<Variant Name>

		Title : POWER_SIGNAL	
ASUSTeK COMPUTER INC.		Engineer: <i>CH/Fred</i>	
Size	Project Name	Rev	
Custom	UL50AT	2.0	
Date: <i>Friday, October 16, 2009</i>		Sheet <i>93</i> of <i>97</i>	





<Variant Name>

		Title : <Title>	
ASUSTeK COMPUTER INC.		Engineer: <i>CH/Fred</i>	
Size	Project Name	Rev	
A	UL50AT	2.0	
Date: <i>Friday, October 16, 2009</i>		Sheet	95 of 97

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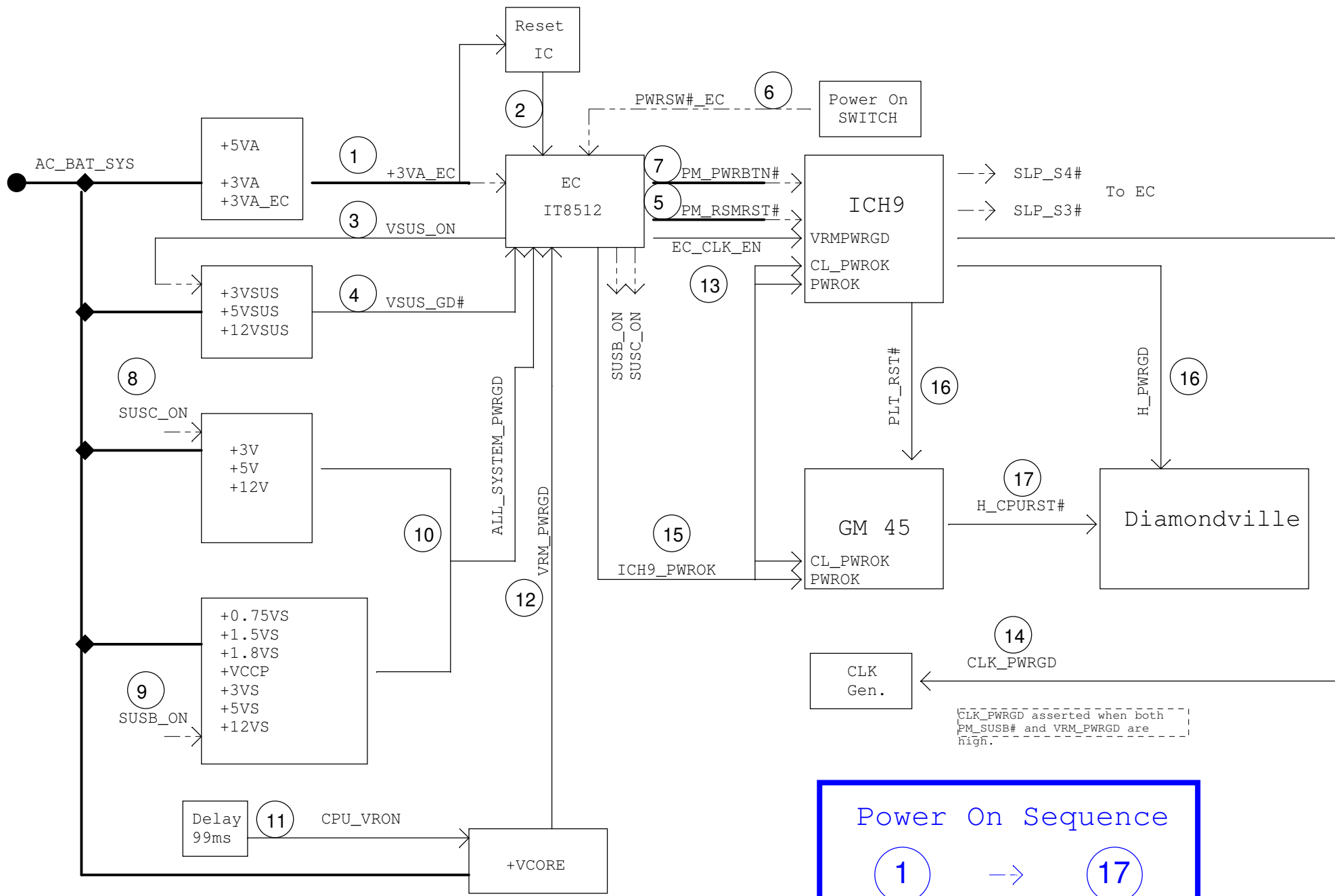
D

D

Rev	Date	Description
1.00		First Release!
1.10		
2.00		

<Variant Name>

		Title : HISTORY
ASUSTeK COMPUTER INC.		Engineer: Jack Hsu
Size Custom	Project Name UL50AT	Rev 2.0
Date: Friday, October 16, 2009		Sheet 96 of 97



<Variant Name>