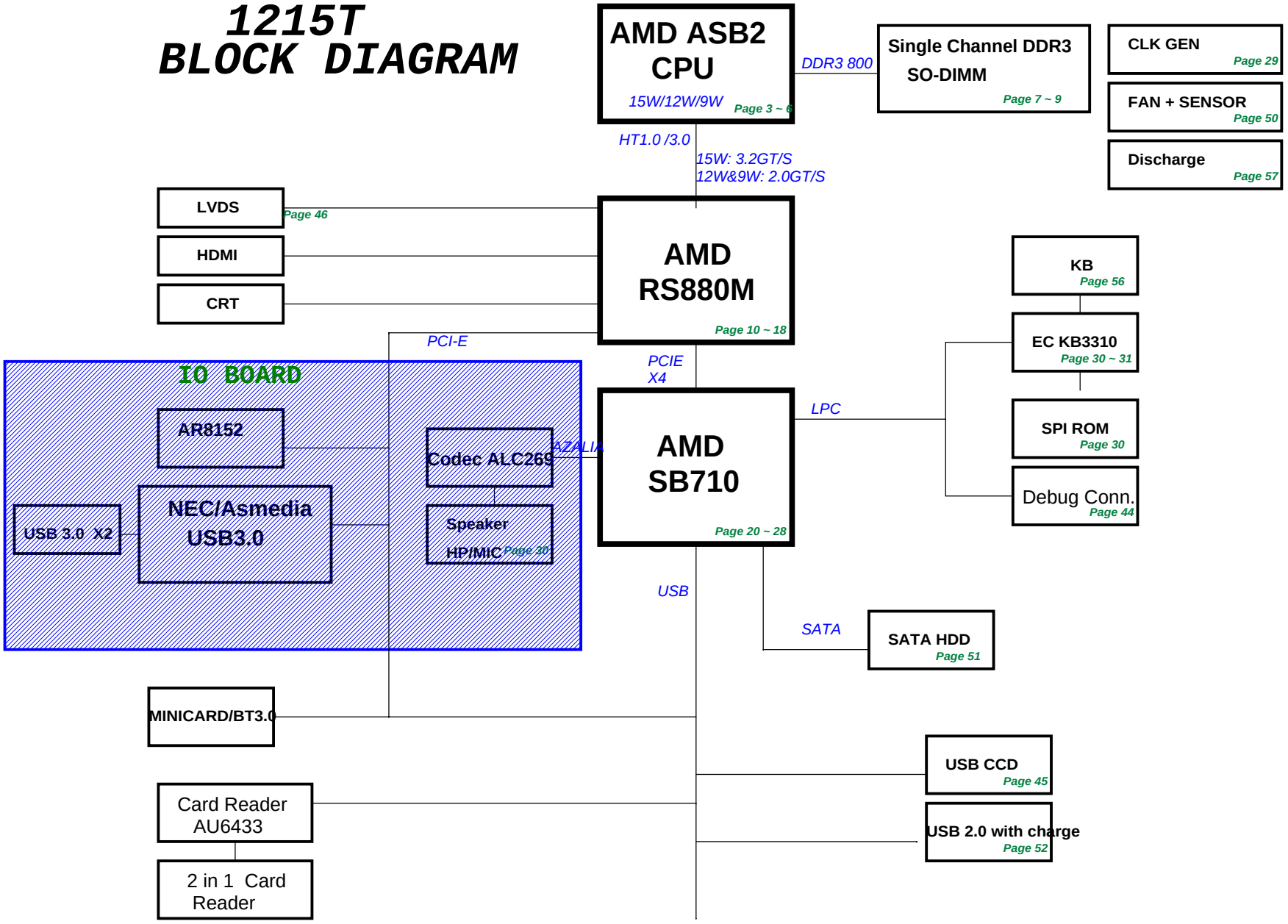
1215T BLOCK DIAGRAM



<Variant Name>

ASUSTeK Computer INC

Title : Block Diagram

Engineer: N/A

Size	Project Name	Rev
Custom	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 1 of 80

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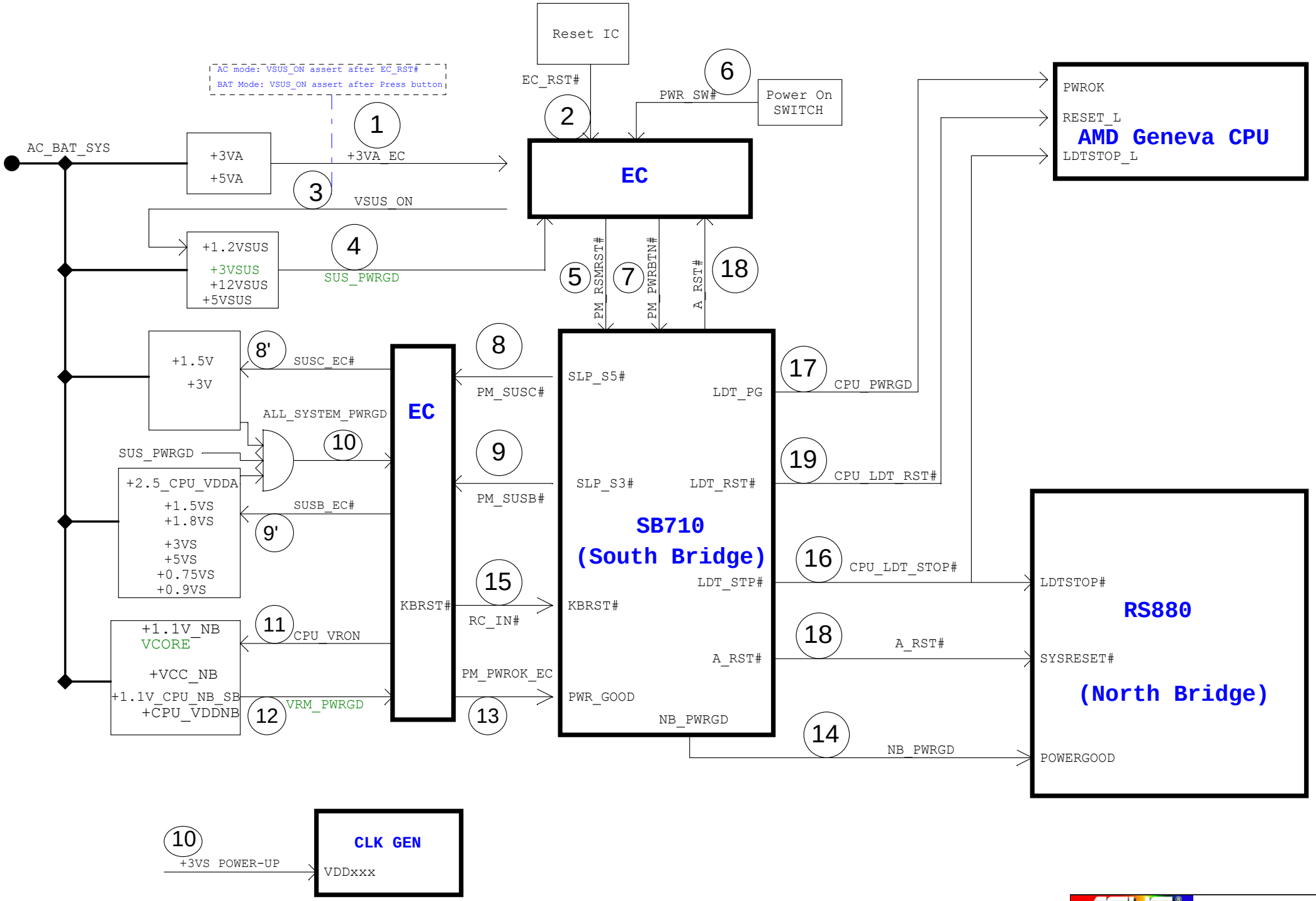
GRATIS - FOR FREE



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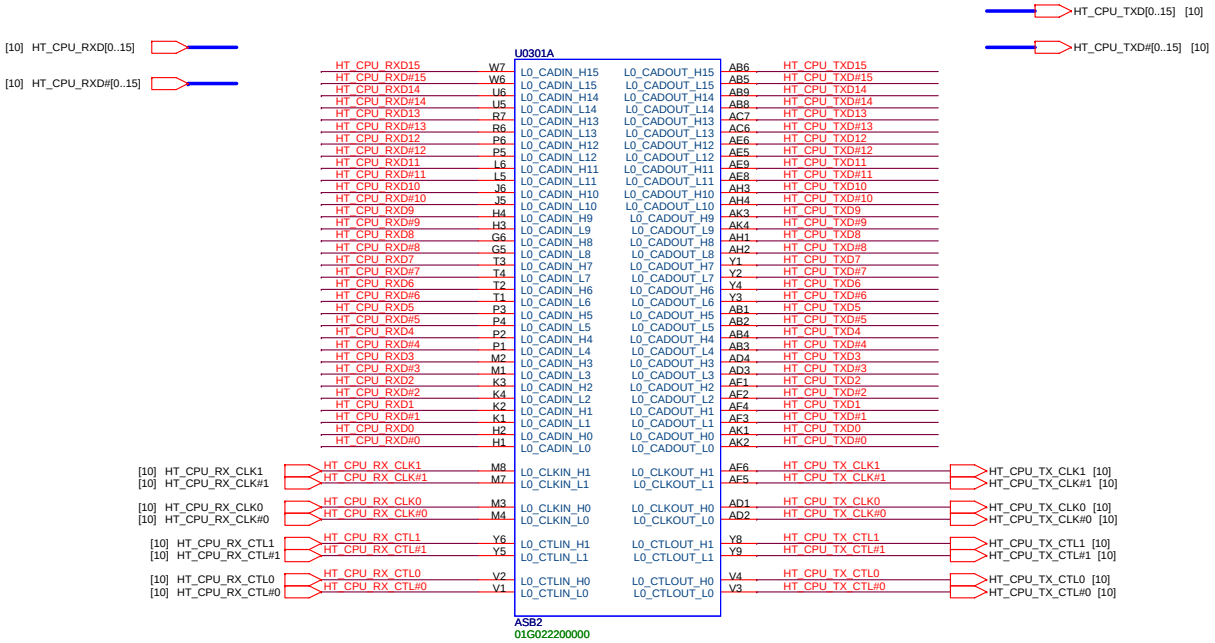
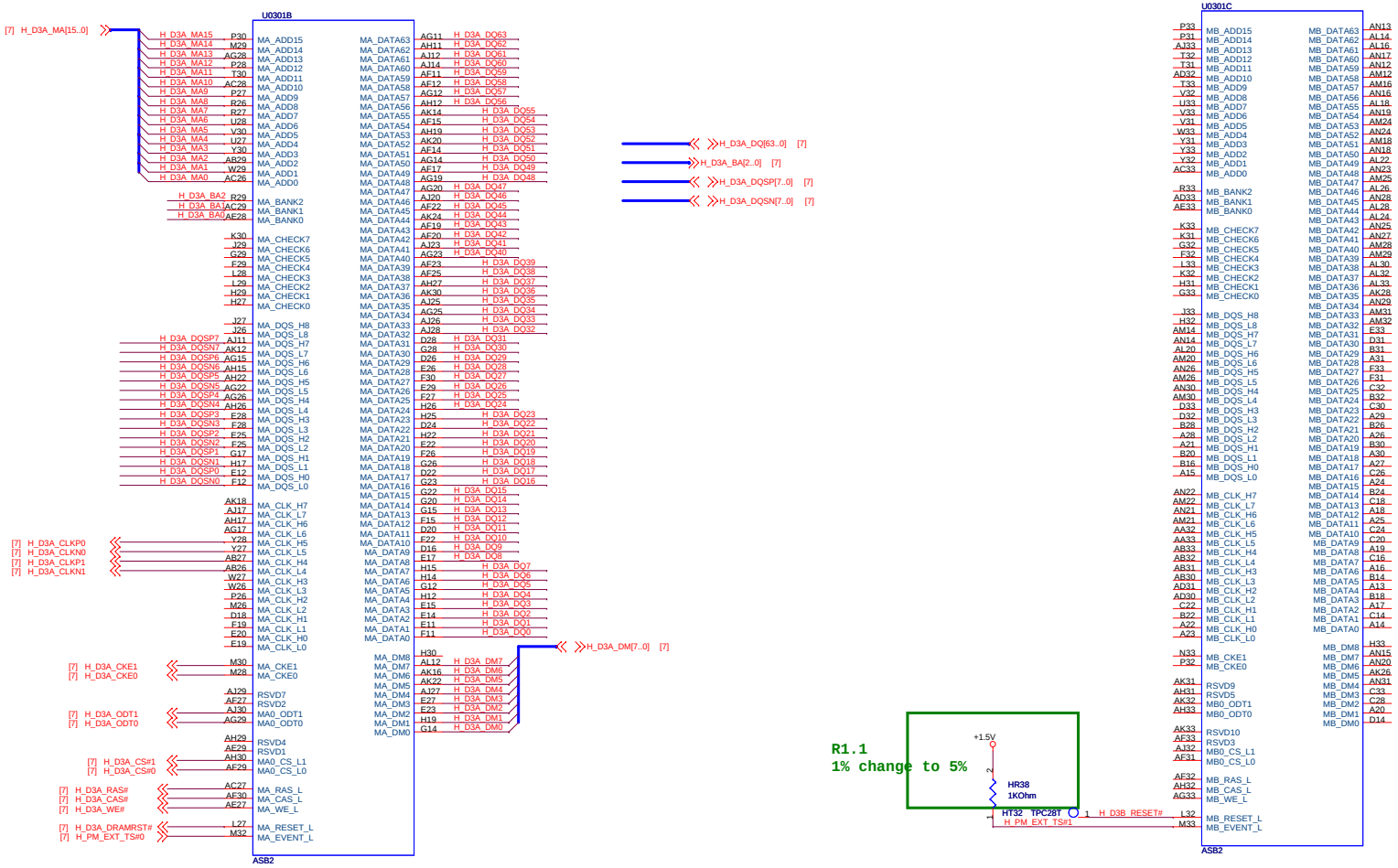
GRATIS - FOR FREE

ASUSTeK.Computer.INC	Title : Power sequence		
	Engineer: N/A		
Size: Custom	Project Name: 1215T		Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 2 of 80		



hexainf@hotmail.com
GRATIS - FOR FREE

ASUSTeK.Computer.INC	Title : Conesus HT I/F	
	Engineer: N/A	
Size: Custom	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 3 of 80	



Change list:

1、CLK 0 and 1 reserved follow AMD Schematic check list。

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GRATIS - FOR FREE

ASUSTeK.Computer.INC	Title : Conesus DDR2 MEM I/F	
	Engineer: N/A	
Size: C	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 4 of 80	

CORE_TYPE	O-IO-S	Indicates that the processor is capable of split Northbridge and core voltage plane operation. If open, the processor requires a unified core and Northbridge voltage plane. If shorted to VSS, split core and Northbridge voltage plan operation is supported.

DEL C0503 at 0414

need check

route as diff pair 5/5/5,10mil

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

for warm reset

PROCHOT

EC to CPU/PWR

THRNTRIP

NOTICE r0541

R1.1

NEED CHECK

PLACE THEM CLOSE TO CPU WITHIN 1"

Route as 80ohm, diff

HDT

Debug 箇痙 090405

DRAM Interface Voltage Reference

PLACE CLOSE TO CPU

ACC

follow AMD checklist

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<Variant Name>

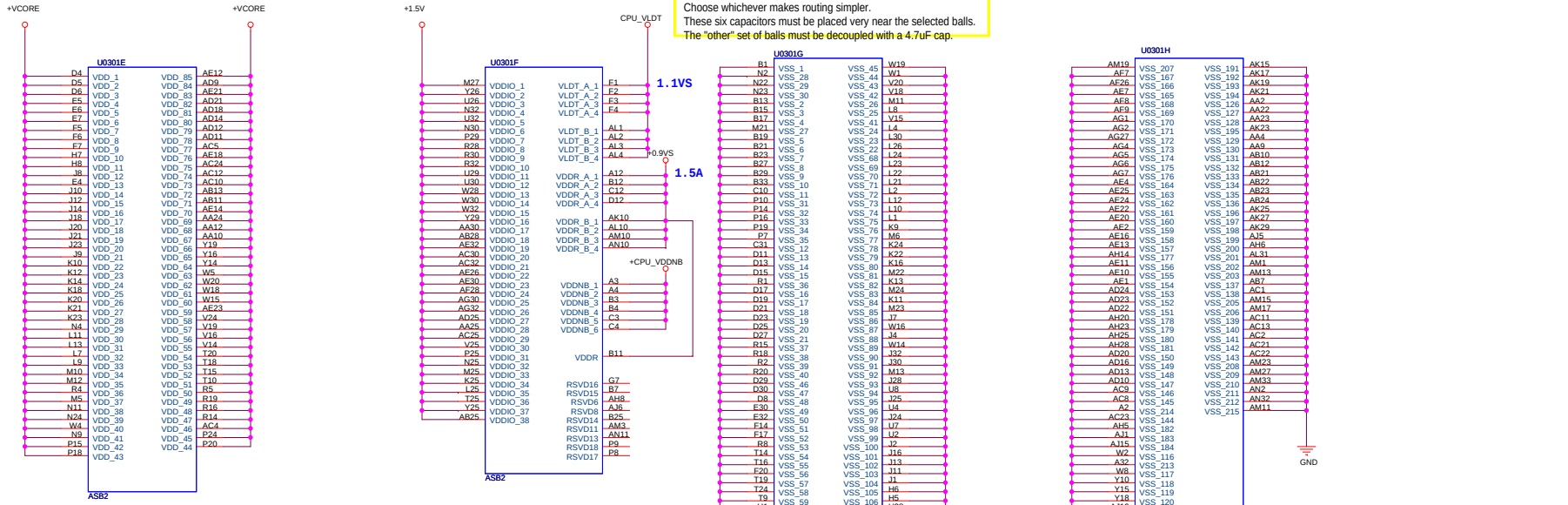
Title Conesus CNT/DBG/THERM

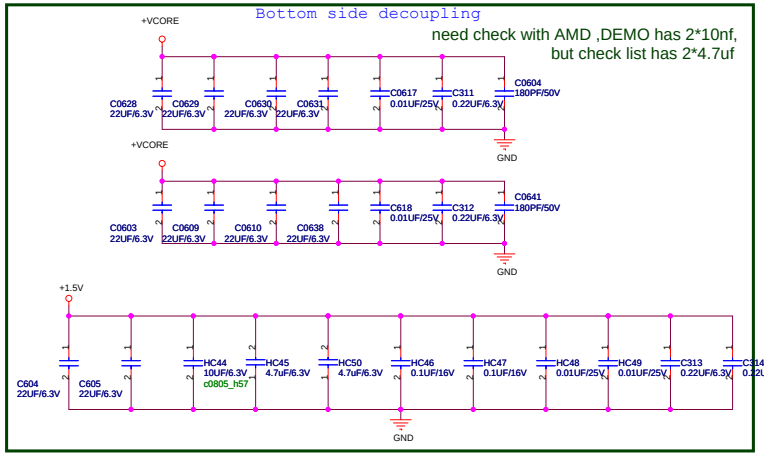
ASUSTeK.Computer.INC

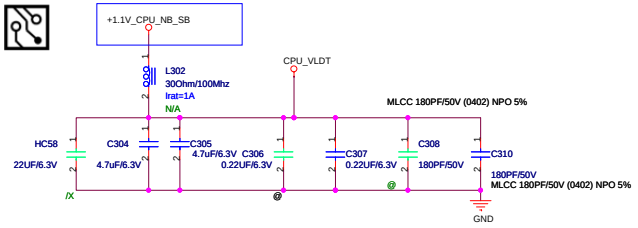
Engineer: N/A

Size	Project Name	Rev
C	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 5 of 80







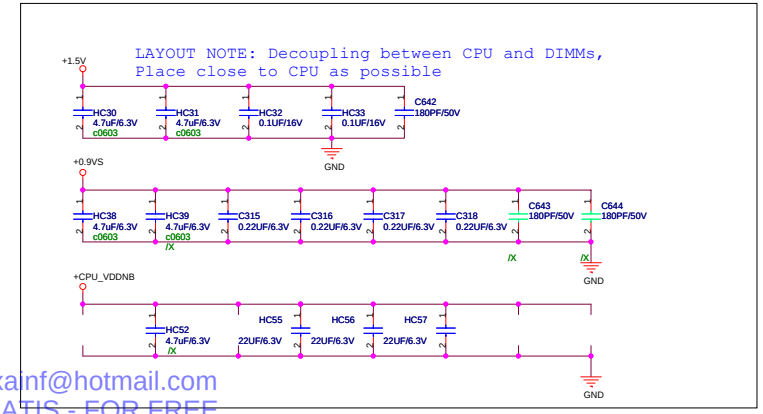


Table 6. Power Supply/Voltage Regulator Interface Pin Descriptions

Signal Name	Type	Description
PSI_L	O-IO-S	Power Status Indicator for the VDD Power Supply regulator. This signal may be used by the regulator to improve efficiency when the processor is in low power states.
VDD	S	Core power supply
VDD_SENSE	A	VDD voltage monitor pin
VDDNB	S	Northbridge power supply
VDDNB_SENSE	A	VDDNB voltage monitor pin
VDDIO	S	DDR SDRAM I/O ring power supply
VDDIO_SENSE	A	VDDIO voltage monitor pin
VDDA	S	Filtered PLL Supply Voltage
VDDR_A, VDDR_B	S	VDDR regulator voltage
VDDR_SENSE	A	VDDR voltage monitor pin
VLDT_A,VLDT_B	S	HyperTransport™ I/O ring power supplies
VLDT_SENSE	A	VLDT voltage monitor pin
VSS	S	Ground
VSS_SENSE	A	VSS voltage monitor pin
SVC	O-IO-S	Serial VID interface clock
SVD	B-IO-OD	Serial VID interface data

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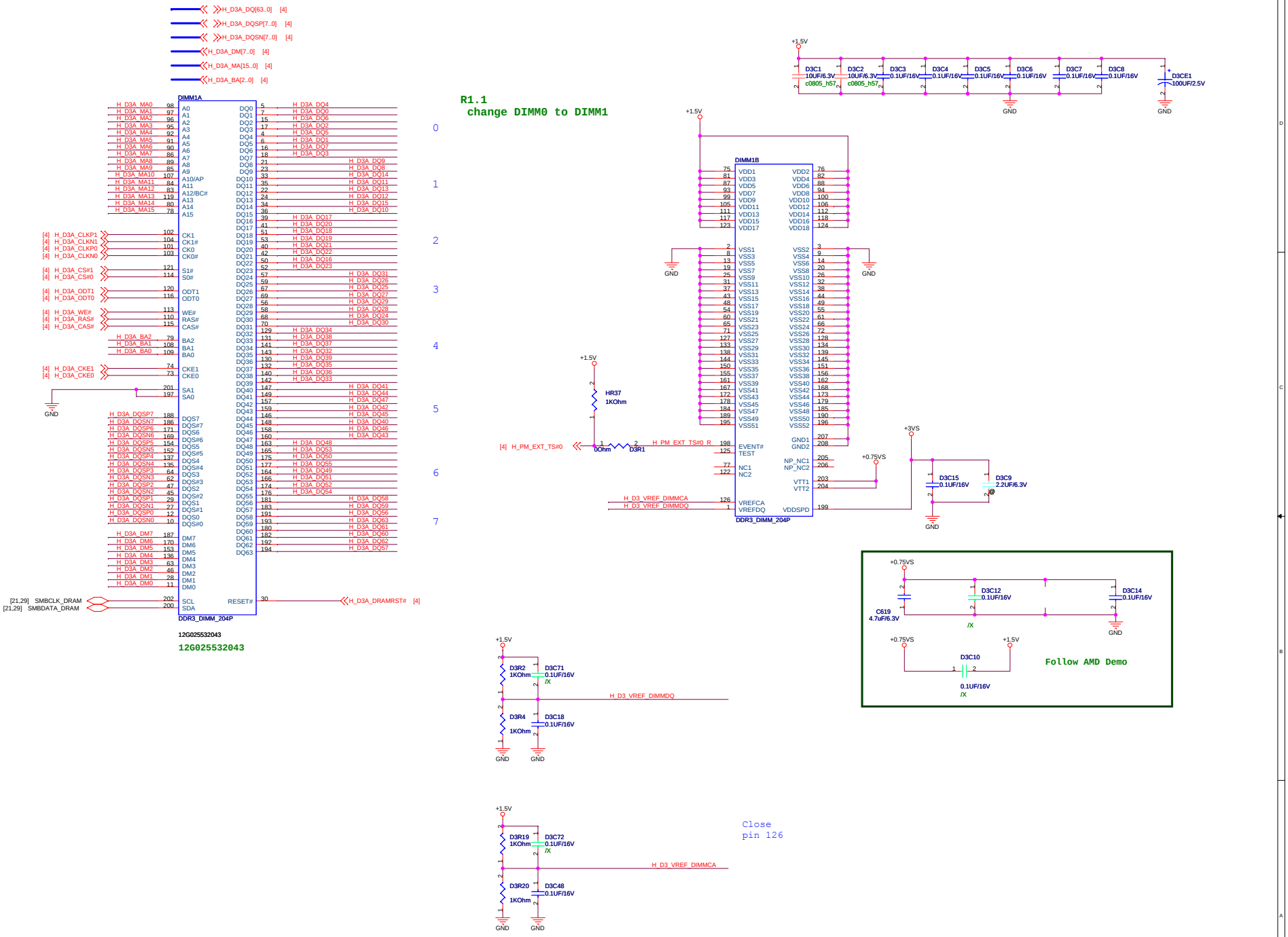
ASUSTeK.Computer.INC

Title : Conesus Power

Engineer: N/A

Size	Project Name	Rev
C	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 6 of 80



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GRATIS - FOR FREE

<variant_name>

ASUSTeK COMPUTER INC

Title : DDR3 SO-DIMM0

Engineer:

Size	Project Name	Rev
C	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 7 of 80

<Variant Name>

Title : DDR2 SO-DIMM1

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 8 of 80

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Title : DDR2_TERMINATIONS

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 9 of 80

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Signal	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP HT_TXCALN	100R	1.21K	301R

Title : RS780M-HT LINK I/F

ASUSTeK.Computer.INC Engineer: N/A

Size	Project Name	Rev
Custom	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 10 of 80

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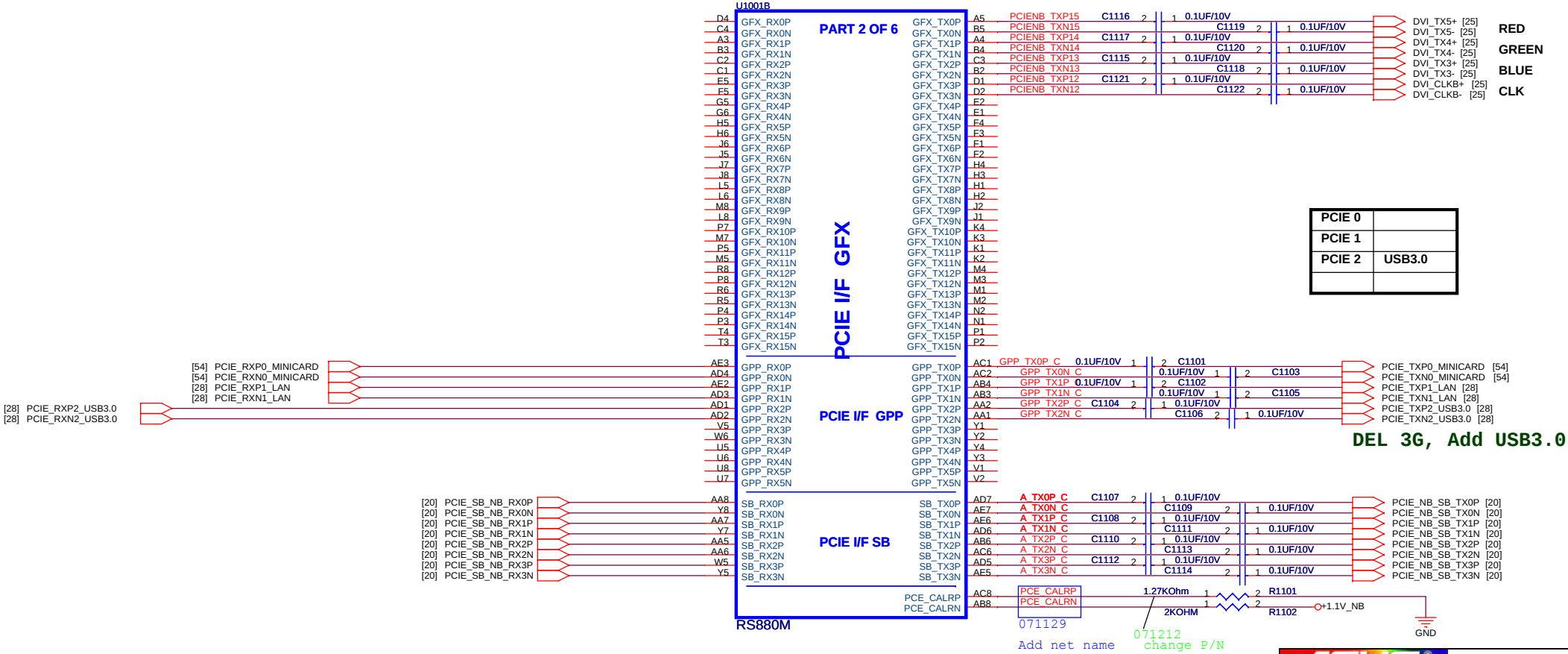
GRATIS - FOR FREE



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notice L1201 L1204 change SL?
090411

09.7.14

080201 R1.1
Change to +1.1V_NB
form NB_VDD_MUX

R1.1 ADD C1210

R2.0080401
Change NB_ALLOW_LDTSTOP to ALLOW_LDTSTOP

STRP_DATA	0	1
VCC_NB	1.0V	1.1V

for HDMI

R1.2 for AMD review

R2.0 change R1210 to1K

071218
for measurement near U1001

DEL serial R

for external graphic?
NEED CHECK

100M FOR ALINK
NEED CHECK

U1001C
RS880M
PART 3 OF 6
CRT/TVOUT
LVTM
PLL PWR
PM
CLOCKs
MIS.

Title :	RS780M-SYS I/F
ASUSTeK.Computer.INC	Engineer: N/A
Size: C	Project Name: 1215T
Rev: 1.0	
Date: Tuesday, August 10, 2010	Sheet 12 of 80

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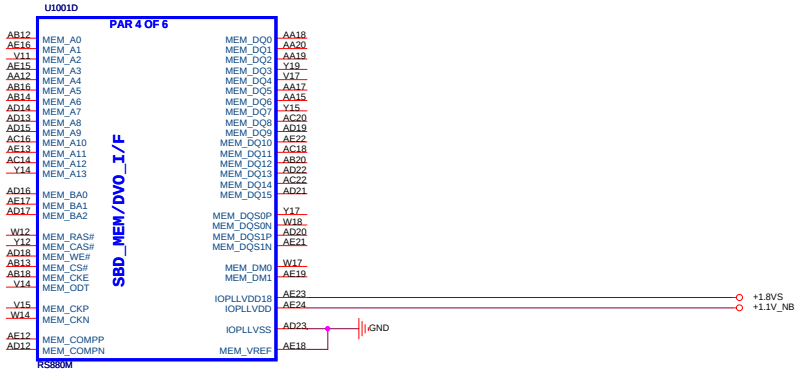
GRATIS - FOR FREE



DFT_GPIO1: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS780:SUS_STAT
```

STRAP_DEBUG_BUS_PCIE_ENABLE

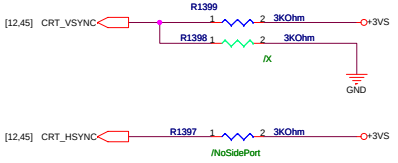
```
Enables the Test Debug Bus using PCIE bus:
1 : Disable ( Can still be enabled using nbcfg register access )
0 : Enable


RS780: configurable thru register setting only
```

RS740/RS780: Enables Side port memory

```
RS780:HSYNC#

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]
```



ASUSTeK.Computer.INC	Title : RS780M-SPMEM/STRAP	
	Engineer: N/A	
Size: C	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 13 of 80	

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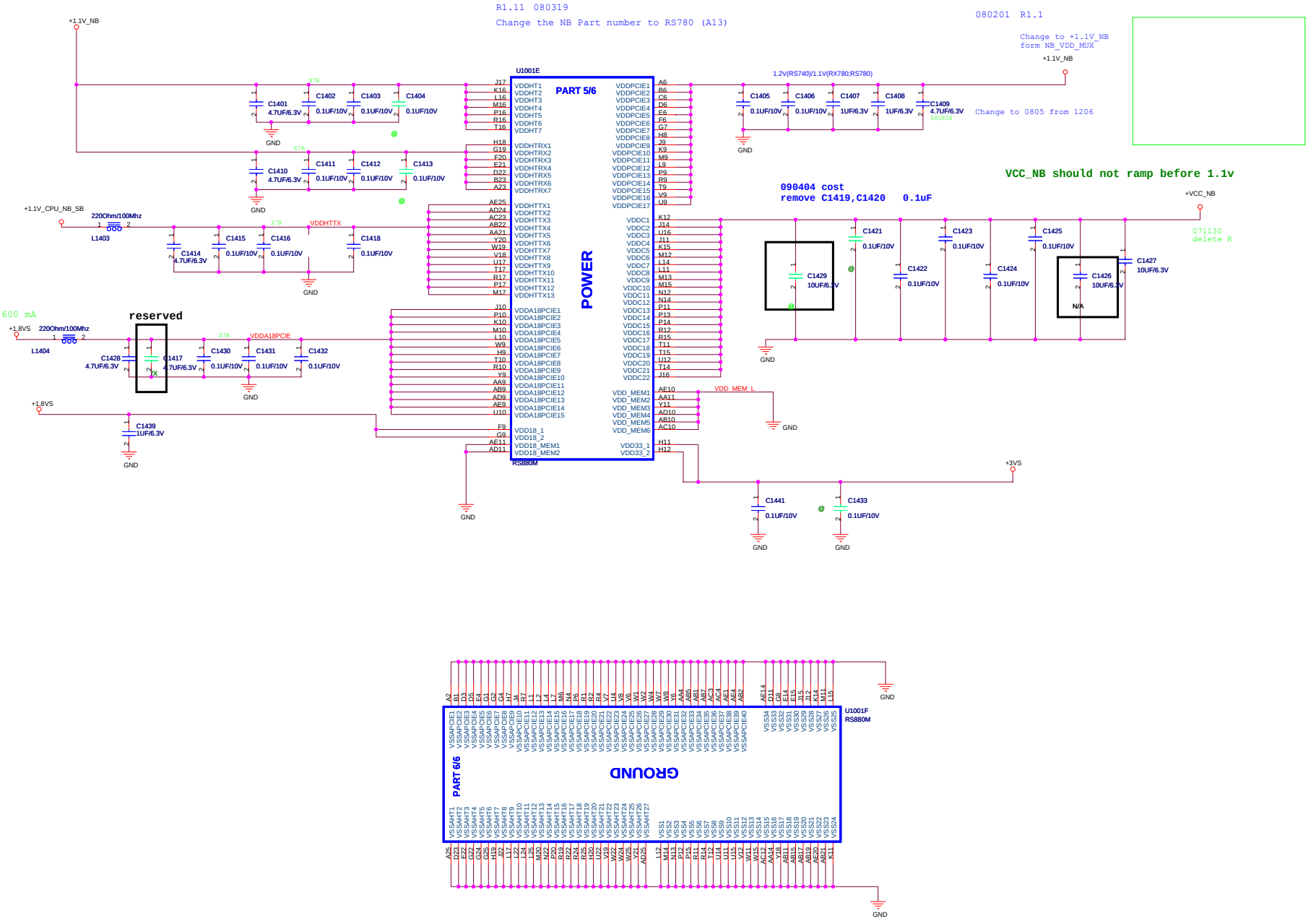
GRATIS - FOR FREE



hexainf@hotmail.com
GRATIS - FOR FREE

ASUSTeK.Computer.INC	Title : RS780M-POWER	
	Engineer: N/A	
Size: C	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 14 of 80	

Check PCIE_RST#

SB700 Part 1 of 5

PCI CLKS

PCI EXPRESS INTERFACE

PCI INTERFACE

CLOCK GENERATOR

LPC

RTC XTAL

CPU

RTC

RTC power.

ACC

change C2015,C2016 to 22pF 090407

R1.1
CHANGE 1% TO 5%

H=1.3 mm

change ctystal (SB710) 07G010413277
090331

2008/0805 Add C2024 for NB_RST# Glitch

S_BATT2

Title : SB700_CPU/PCIE/LPC/CLK

ASUSTeK.Computer.INC

Engineer: N/A

Size: Custom | Project Name: 1215T | Rev: 1.0

Date: Tuesday, August 10, 2010 | Sheet 20 of 80

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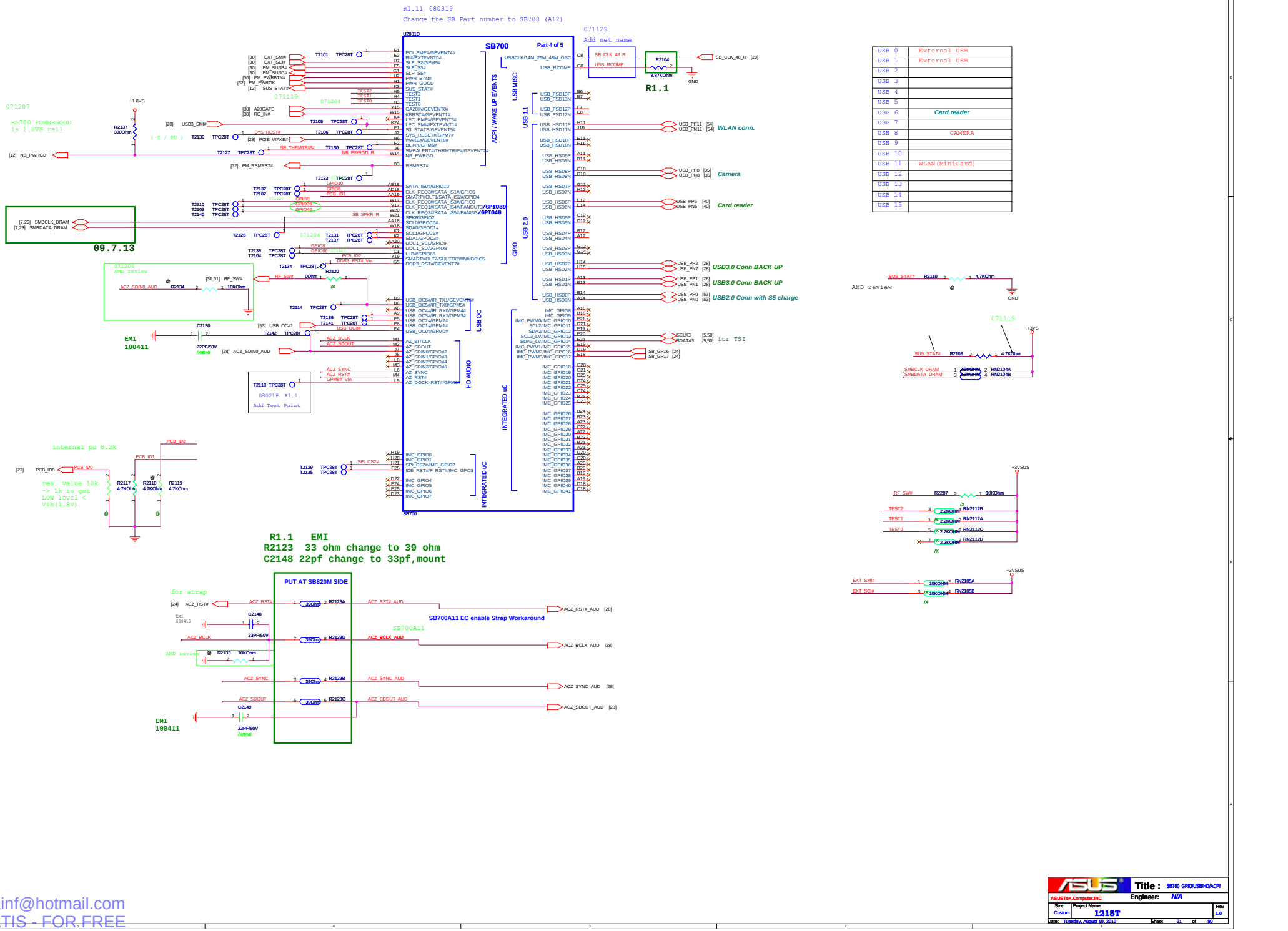
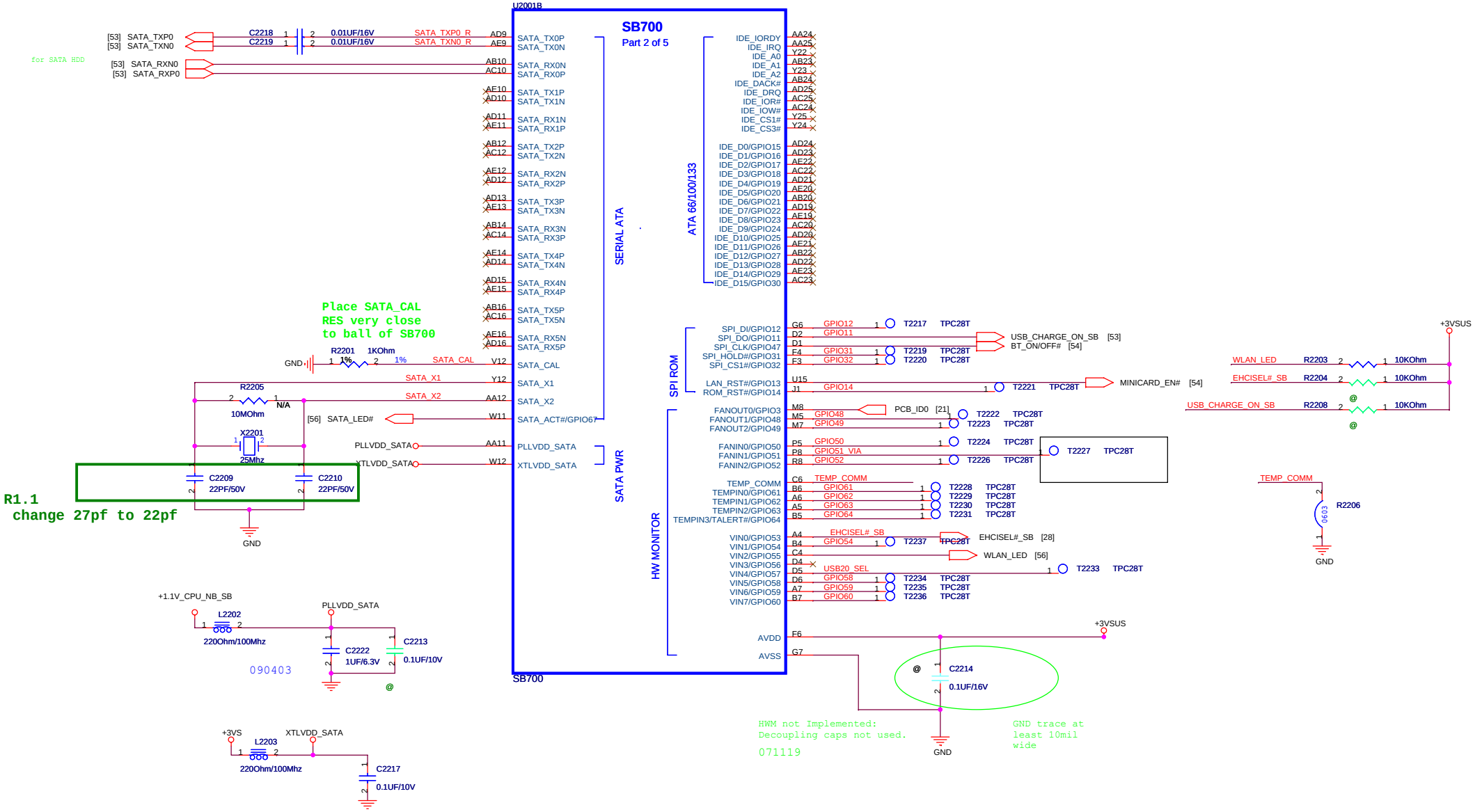


hexainf@hotmail.com
GRATIS - FOR FREE

Change the SB Part number to SB710 (A14)



hexainf@hotmail.com
GRATIS - FOR FREE

<Variant Name>

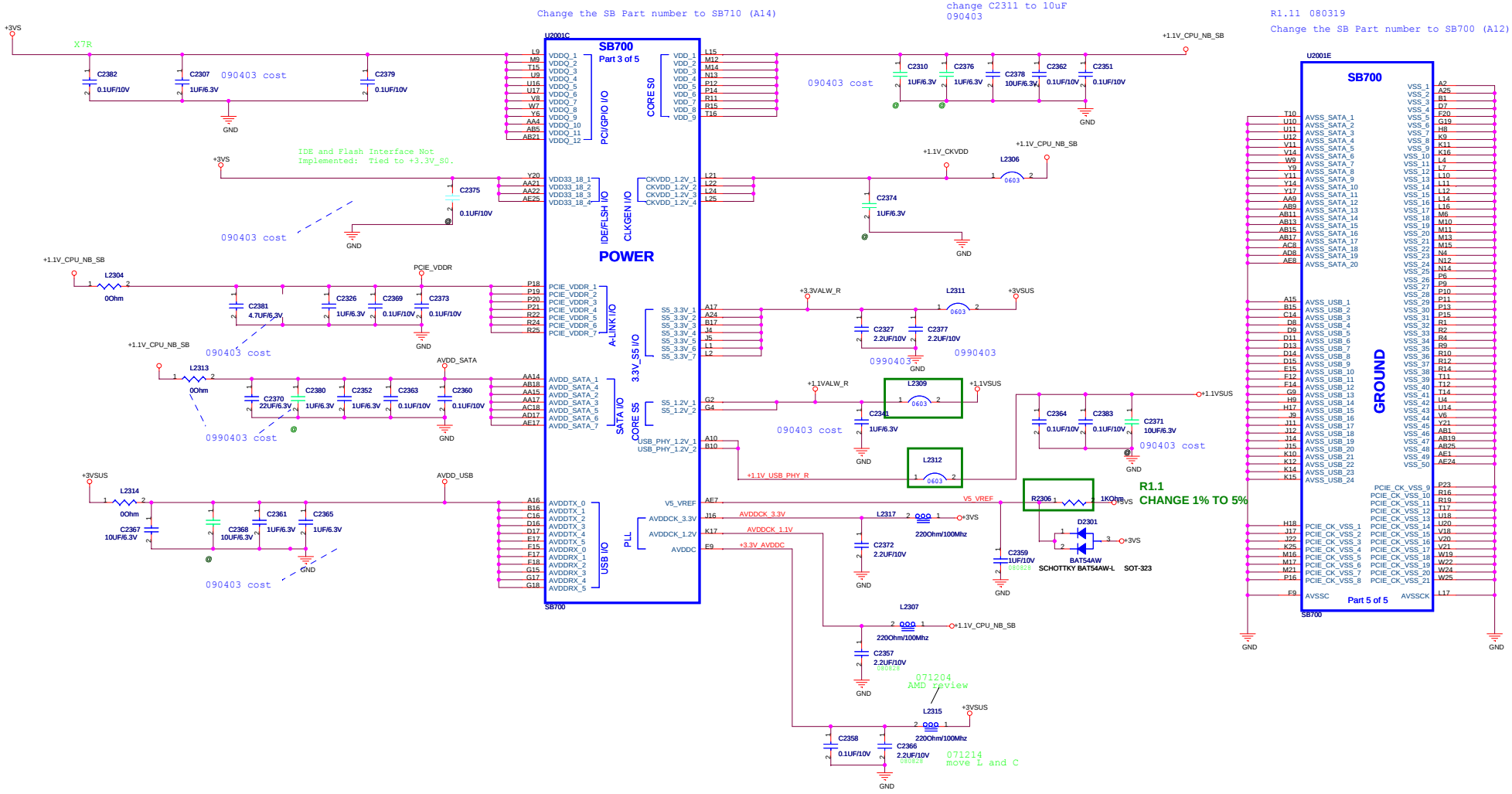
Title : SB700_PATA/SATA

ASUSTeK.Computer.INC

Engineer: N/A

Size	Project Name	Rev
Custom	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 22 of 80



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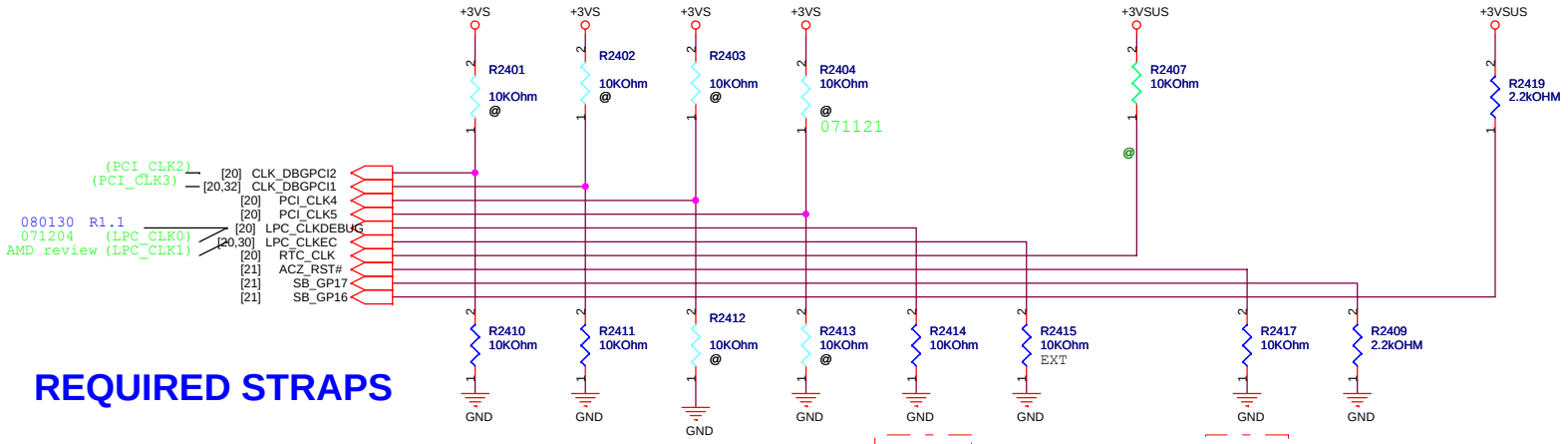
Remove R2405, R2406,R2416
R2408, R2418, R2420, R2418 090405

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	ACZ_RST#	GP17 GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	EC ENABLED	CLKGEN ENABLED	INTERNAL RTC DEFAULT	ENABLE PCI MEM BOOT	H,H = Reserved H,L = SPI ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI MEM BOOT DEFAULT	L,H = LPC ROM (Default) L,L = FWH ROM

For SB700 A12 and later version

080204 R1.1
Change the Text Comment

<Variant Name>

ASUSTeK.Computer.INC	Title : SB700_STRAP	
	Engineer: N/A	
Size: Custom	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 24 of 80	

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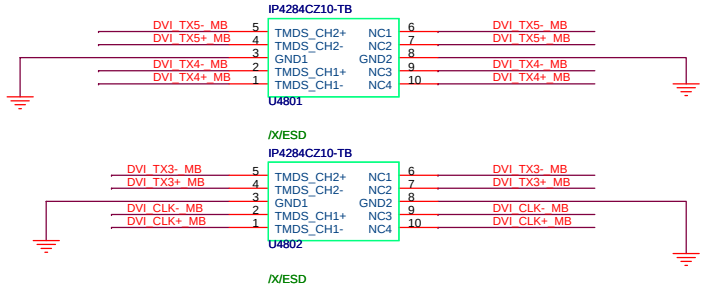
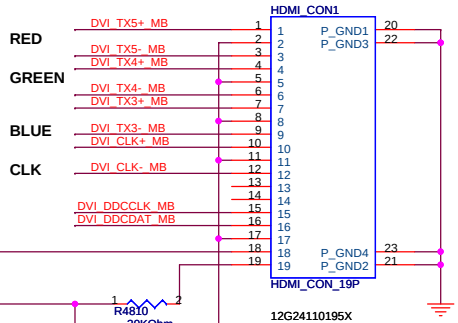
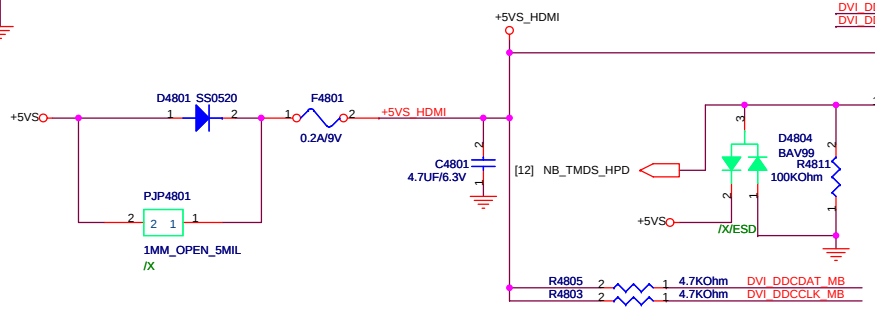
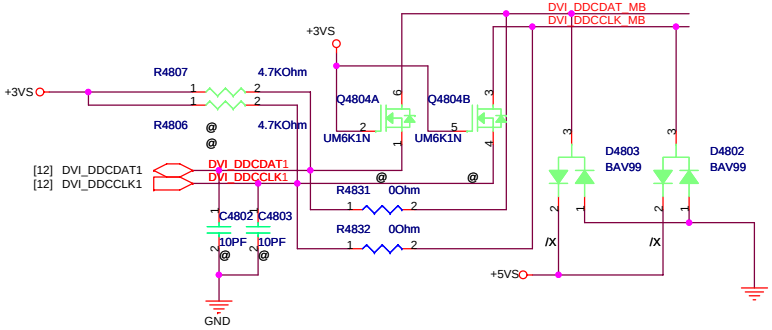
Close to HDMI CON(ESD Protection)

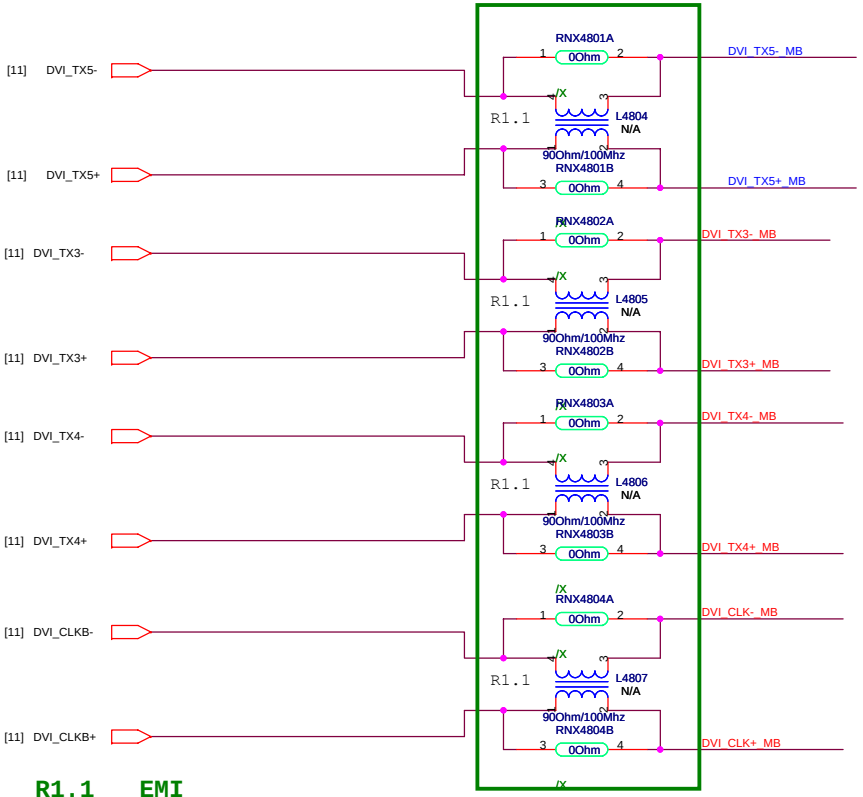


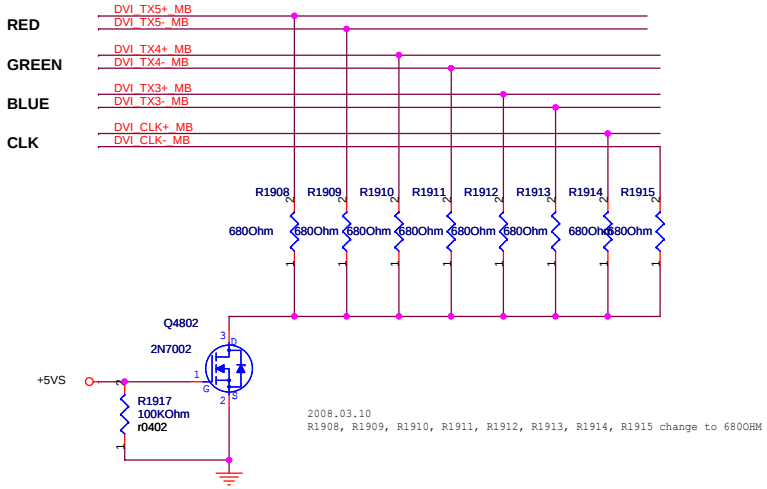
HDMI CON











2008.03.10
R1908, R1909, R1910, R1911, R1912, R1913, R1914, R1915 change to 680OHM

R1.1 EMI
mount choke,unmount o ohm resistor

<Variant Name>

ASUSTek COMPUTER INC

Title : HDMI

Engineer: N/A

Size	Project Name	Rev
Custom	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 25 of 80

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GRATIS - FOR FREE

<Variant Name>

ASUSTek Computer INC.	Title : Bluetooth	
	Engineer: N/A	
Size: A	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 27 of 80	

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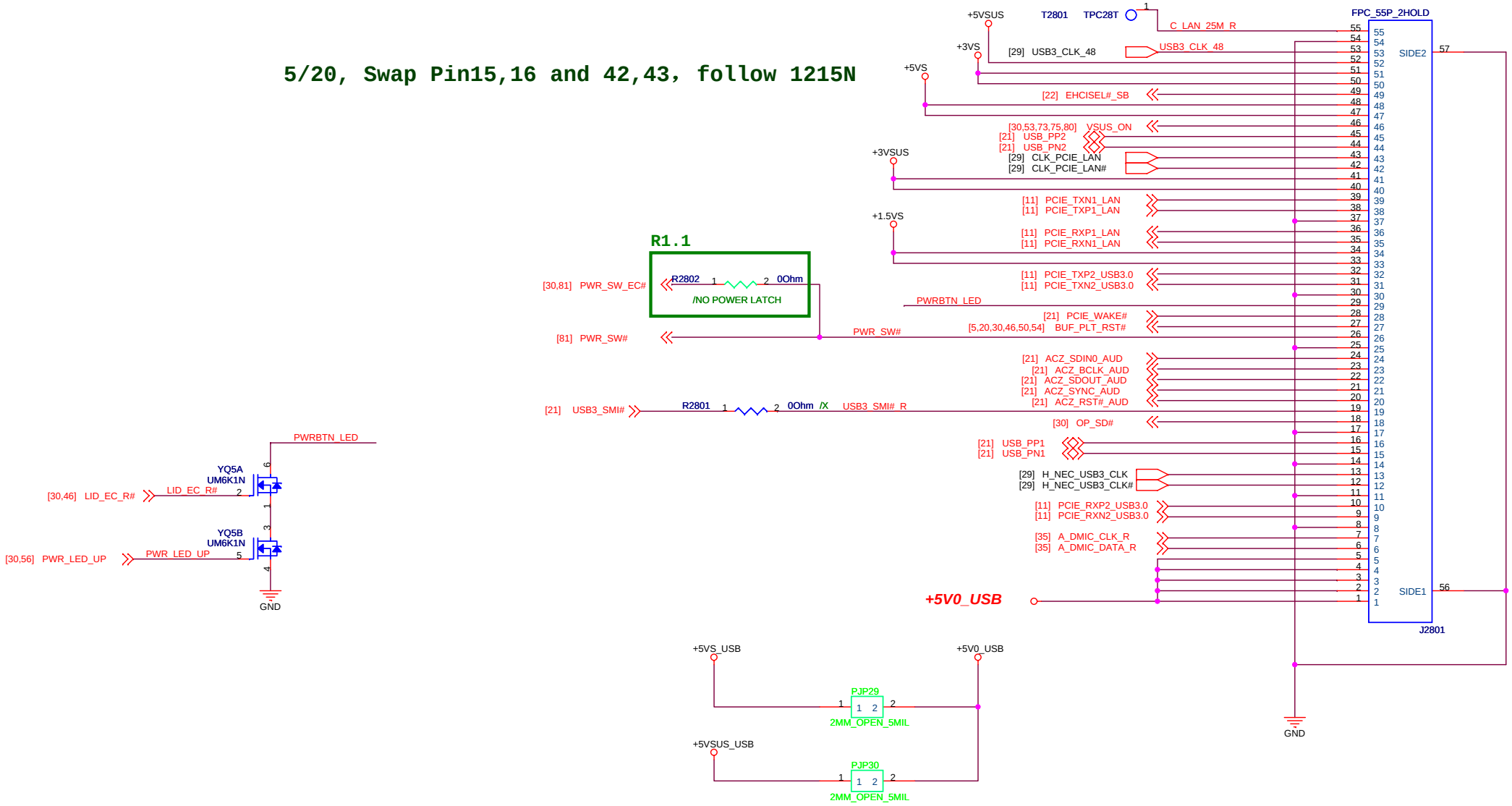
GRATIS - FOR FREE



<Variant Name>

Title : Small brd Conn

ASUSTek Computer INC. Engineer: N/A

Size	Project Name	Rev
B	1215T	1.0

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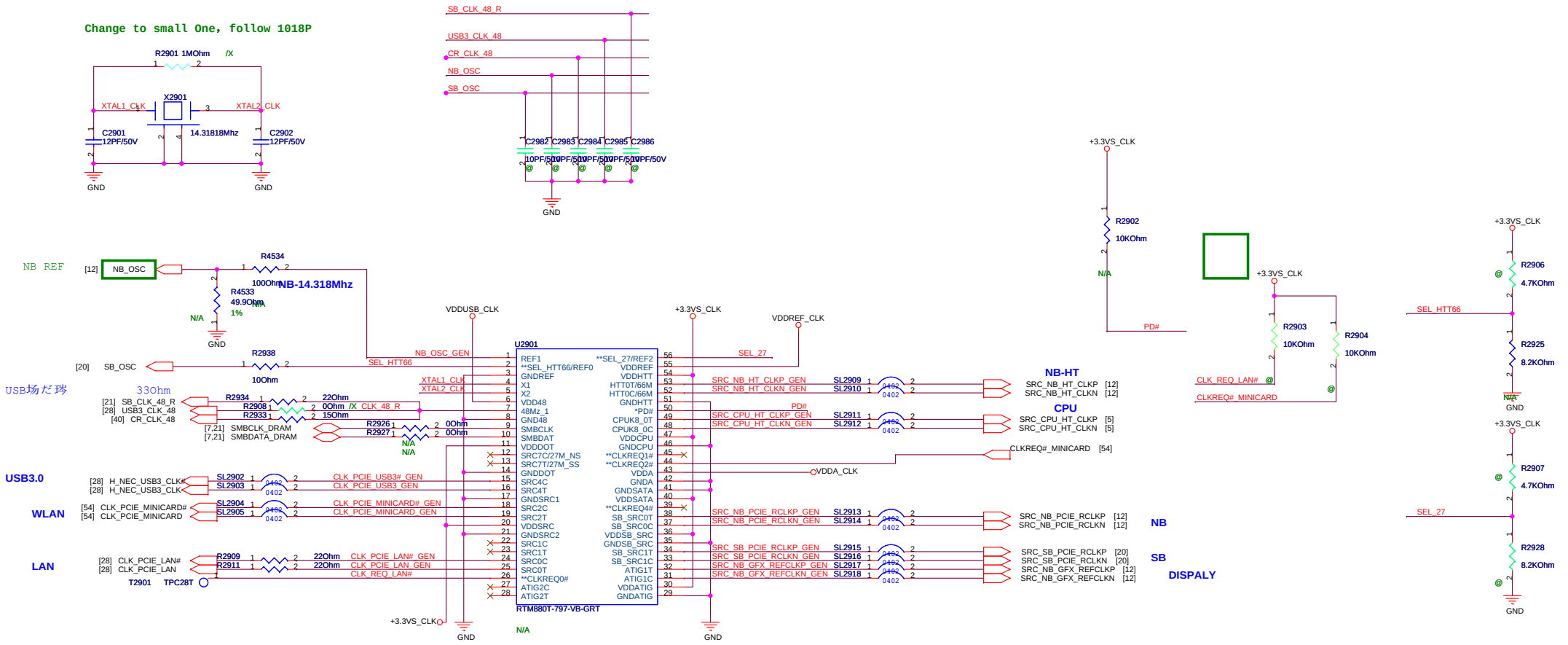

SEL_27		
	0	100 MHz differential spreading SRC clock
	1	27MHz non-spreading singled clock on pin12 27MHz spread clock on pin13.

SEL_HTT66		
	0	100 MHz differential HTT clock
	1	66MHz 3.3V single ended HTT clock

<Variant Name>

ASUSTeK COMPUTER INC

Title : RTM880T-797-VB-GRT

Engineer: N/A

Size	Project Name	Rev
Custom	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 29 of 80

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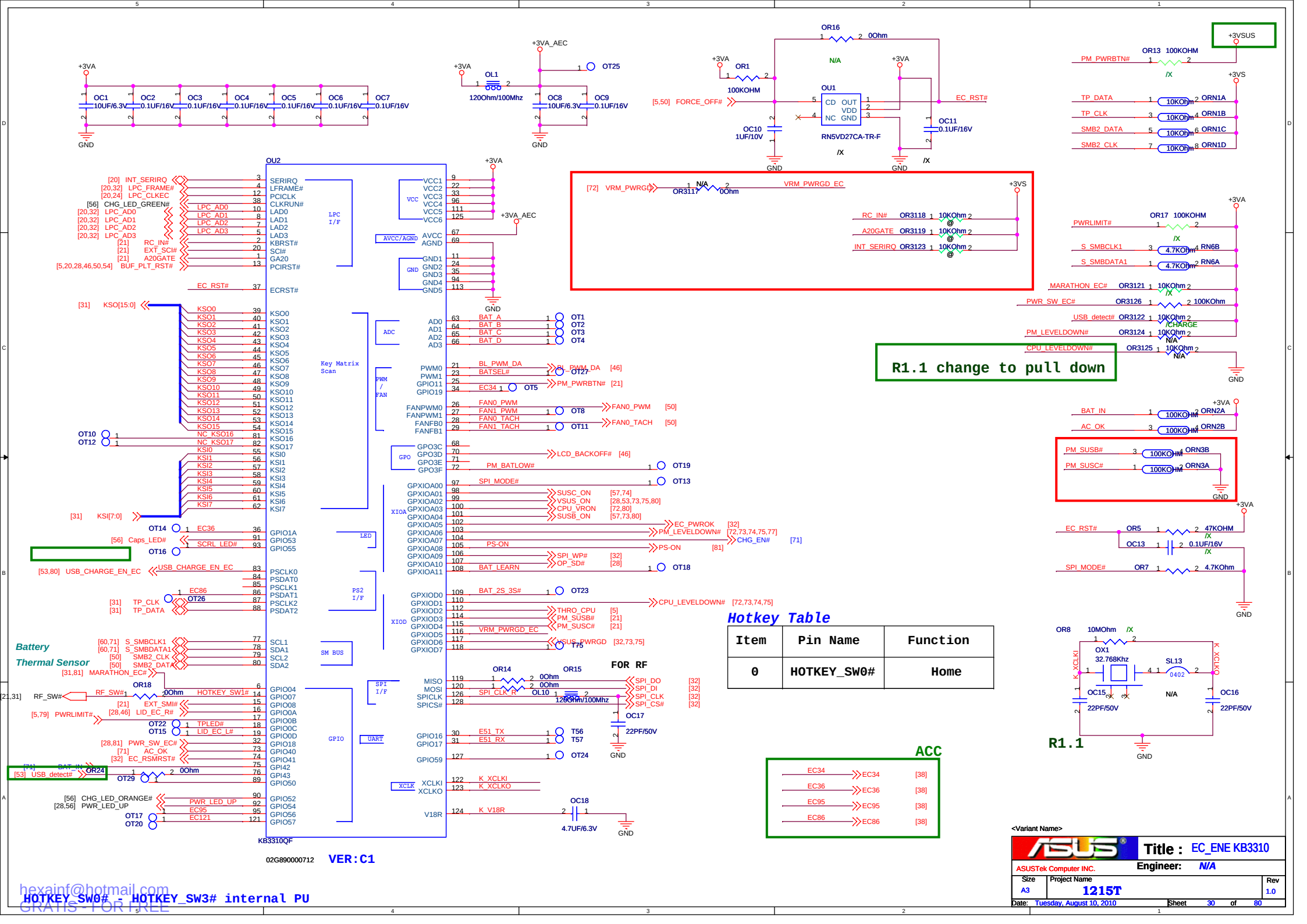
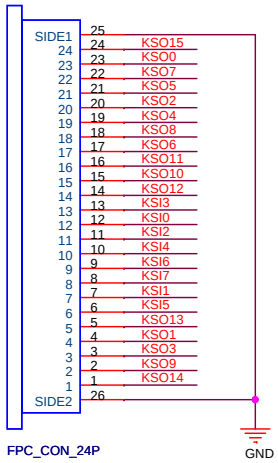

OU2
KB3310QF
02G890000712
VER:C1
R1.1 change to pull down
Hotkey Table
Item | Pin Name | Function
0 | HOTKEY_SW0# | Home
FOR RF
ACC
Battery
Thermal Sensor
HOTKEY_SW0# - HOTKEY_SW3# internal PU
R1.1
Title : EC_ENE KB3310
ASUSTek Computer INC.
Engineer: N/A
Size A3
Project Name 1215T
Rev 1.0
Date: Tuesday, August 10, 2010
Sheet 30 of 80
hexainf@hotmail.com
GRATIS - FOR FREE

follow 1201T

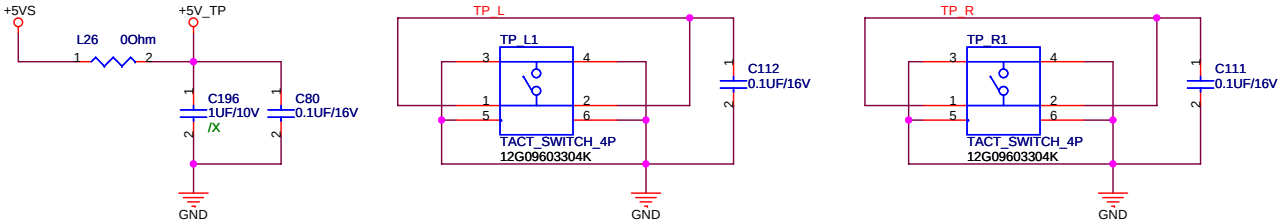
KB_CON1 12G182102402



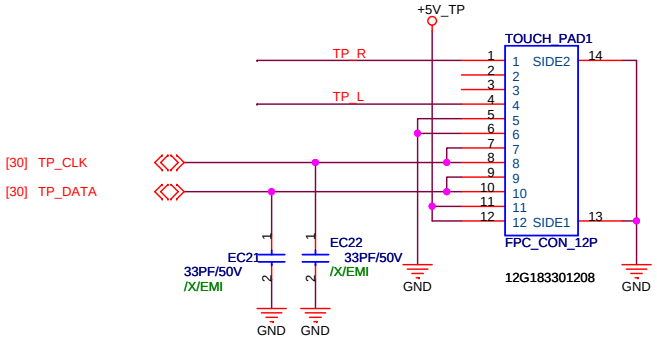
FPC_CON_24P

GND

For Keyboard Connector

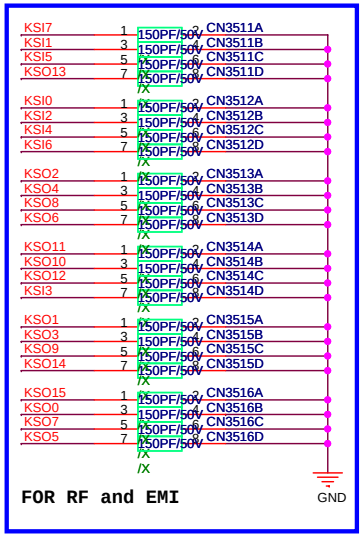


For Touch-Pad



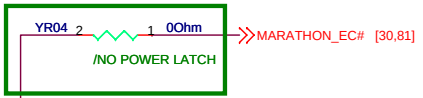
KSO[15:0] [30]

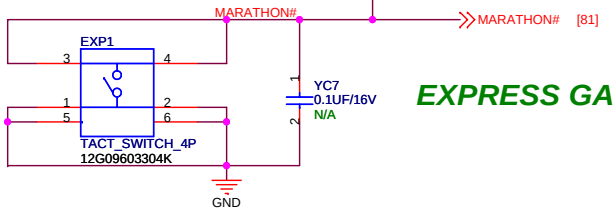
KSI[7:0] [30]



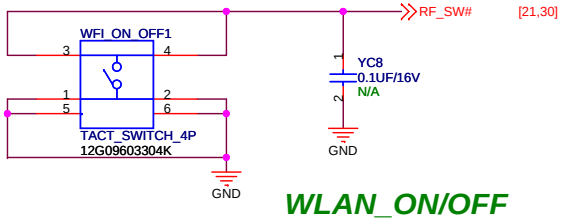
FOR RF and EMI

R1.1





EXPRESS GATE & SHE



WLAN_ON/OFF

R1.1
DEL PWR1

<Variant Name>

ASUSTek Computer INC.	Title : KB_Touch Pad	
	Engineer: N/A	
Size: B	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 31 of 80	

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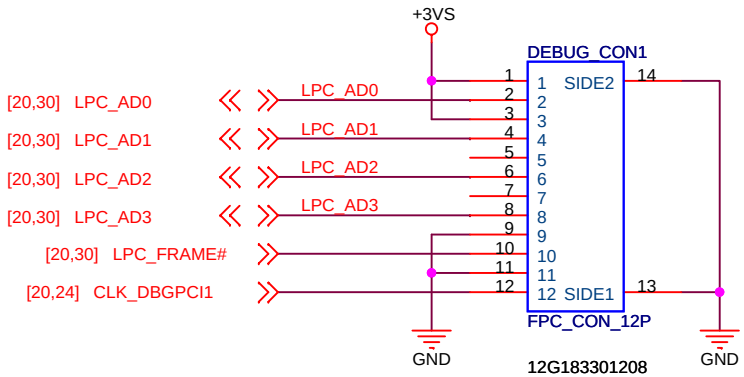
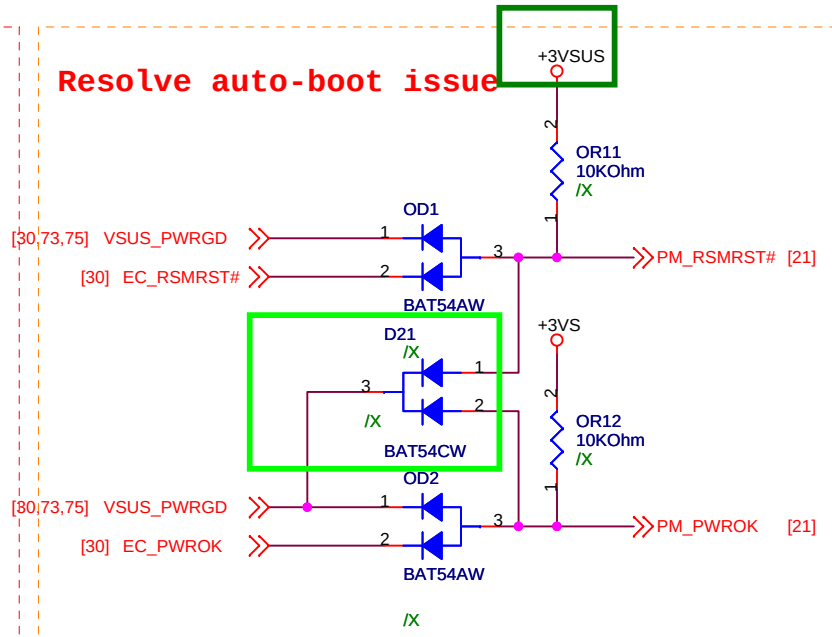
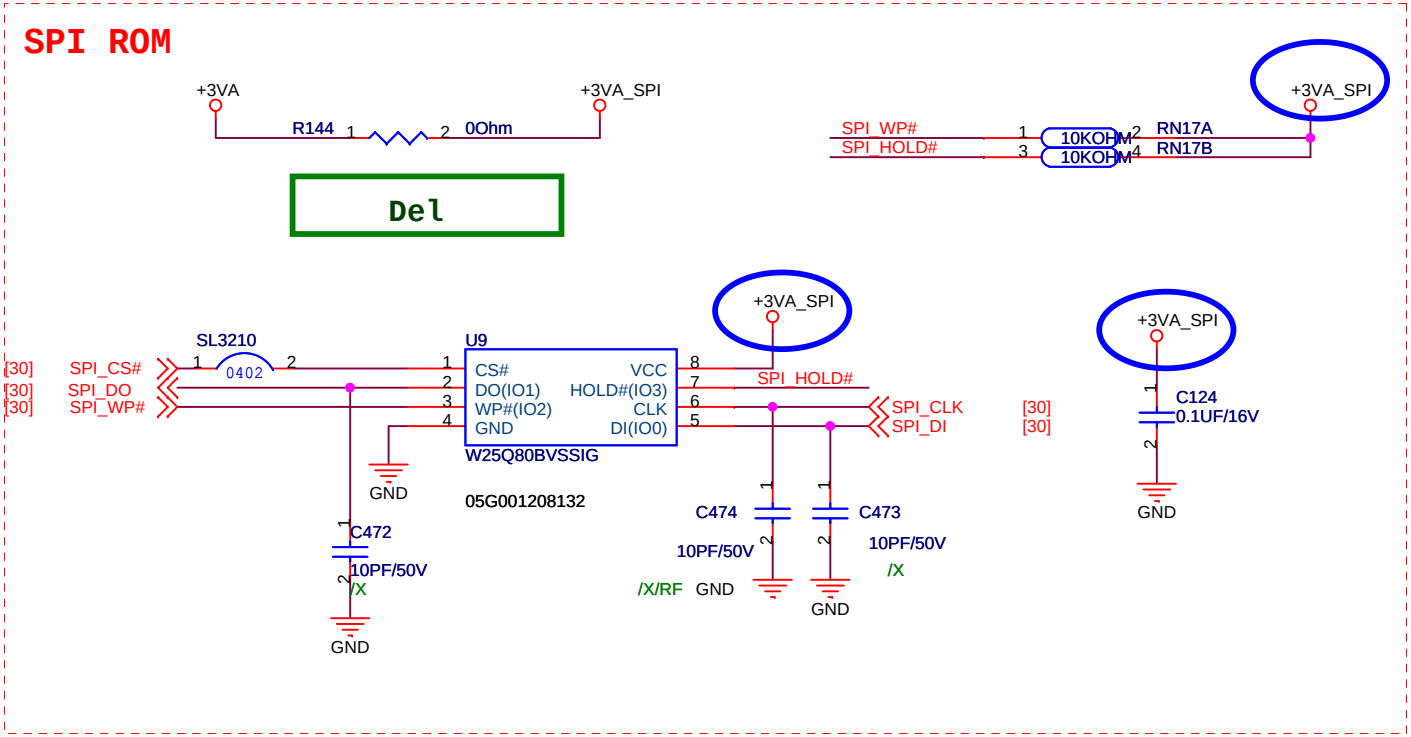
For Debug

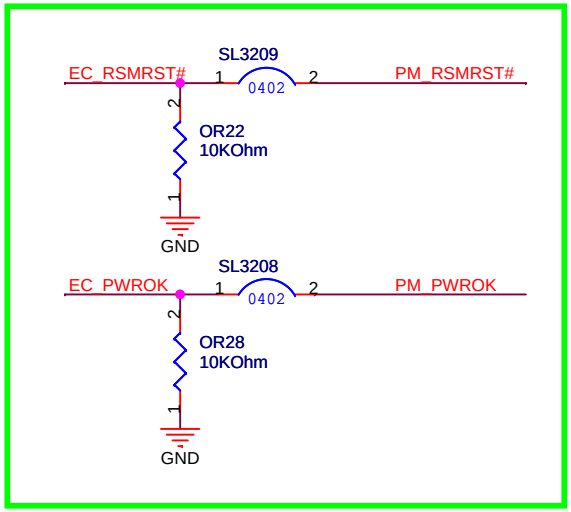


Resolve auto-boot issue



SPI ROM





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<Variant Name>

ASUSTek Computer INC.	Title : SPI ROM/ Debug	
	Engineer: N/A	
Size: A4	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 32 of 80	

<Variant Name>

ASUSTek Computer INC	Title : AR8113/AR8132	
	Engineer: N/A	
Size: A3	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 33 of 80	

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<Variant Name>

ASUSTek Computer INC.

Title : RJ45

Engineer: N/A

Size	Project Name	Rev
A3	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 34 of 80

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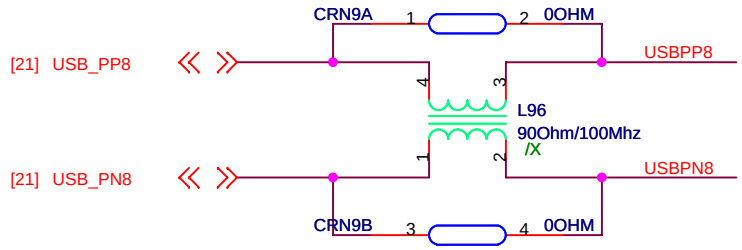

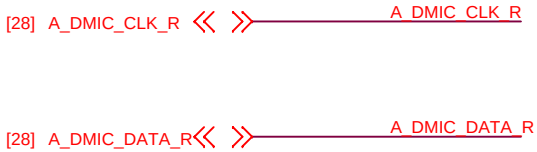

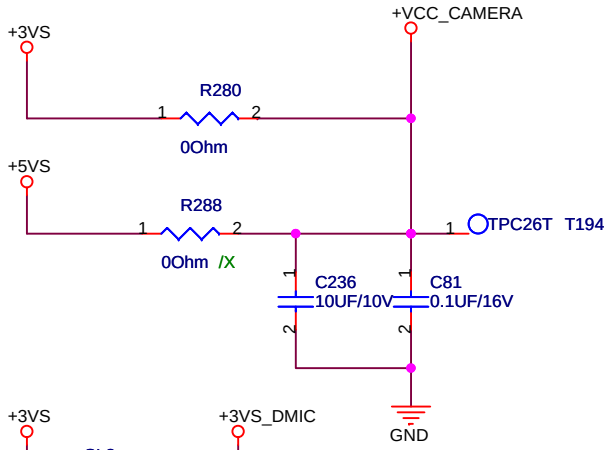

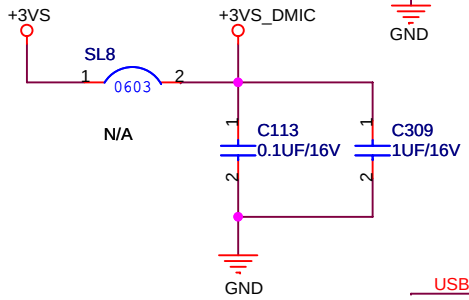

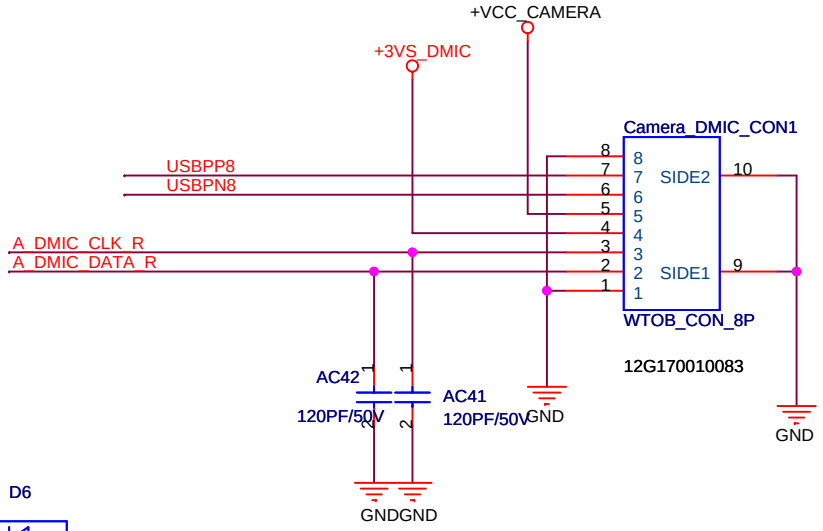

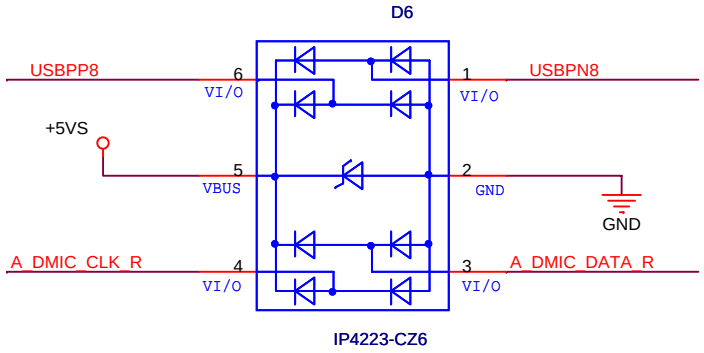

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GRATIS - FOR FREE

<Variant Name>

ASUSTek Computer INC.	Title : CMOS	
	Engineer: N/A	
Size: A4	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 35 of 80	

NOTE
VA6:02G611005006
VB5:02G611005015

<Variant Name>

ASUSTek Computer INC.	Title : ALC269	
	Engineer: N/A	
Size: A	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 36 of 80	

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<Variant Name>

ASUSTek Computer INC.	Title : MIC_HP_SPK	
	Engineer: N/A	
Size: A	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 37 of 80	

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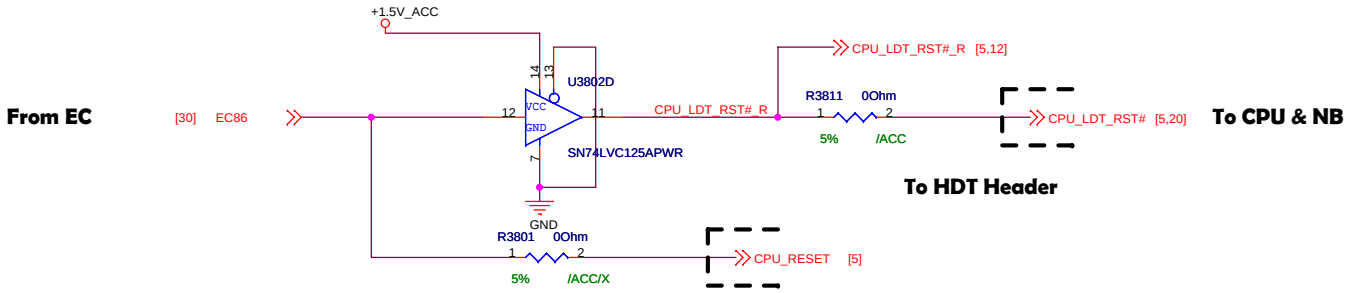
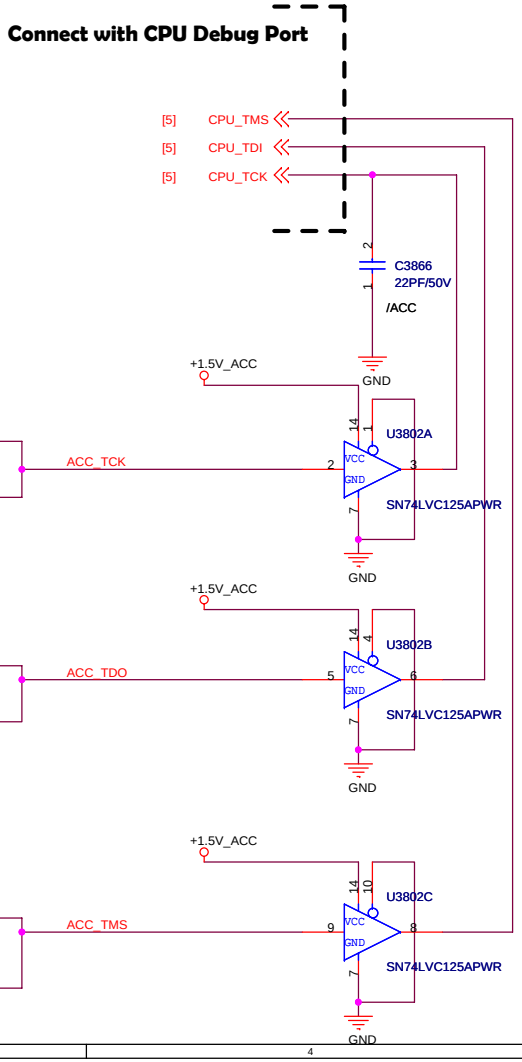
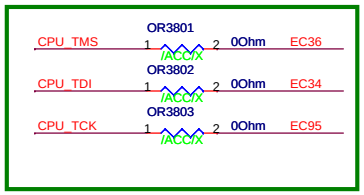
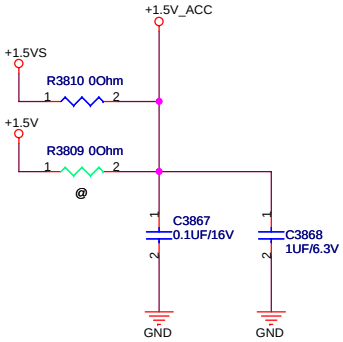
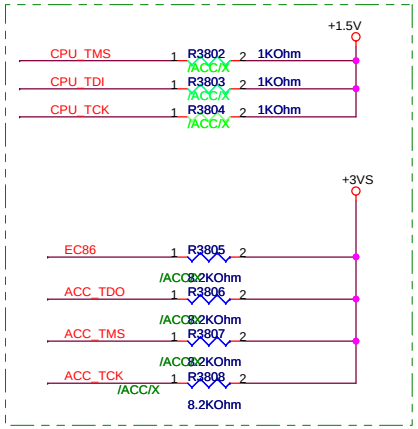
AOD ACC Function











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ASUSTek Computer INC.	Title : ACC	
	Engineer: N/A	
Size: Custom	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 38 of 70	

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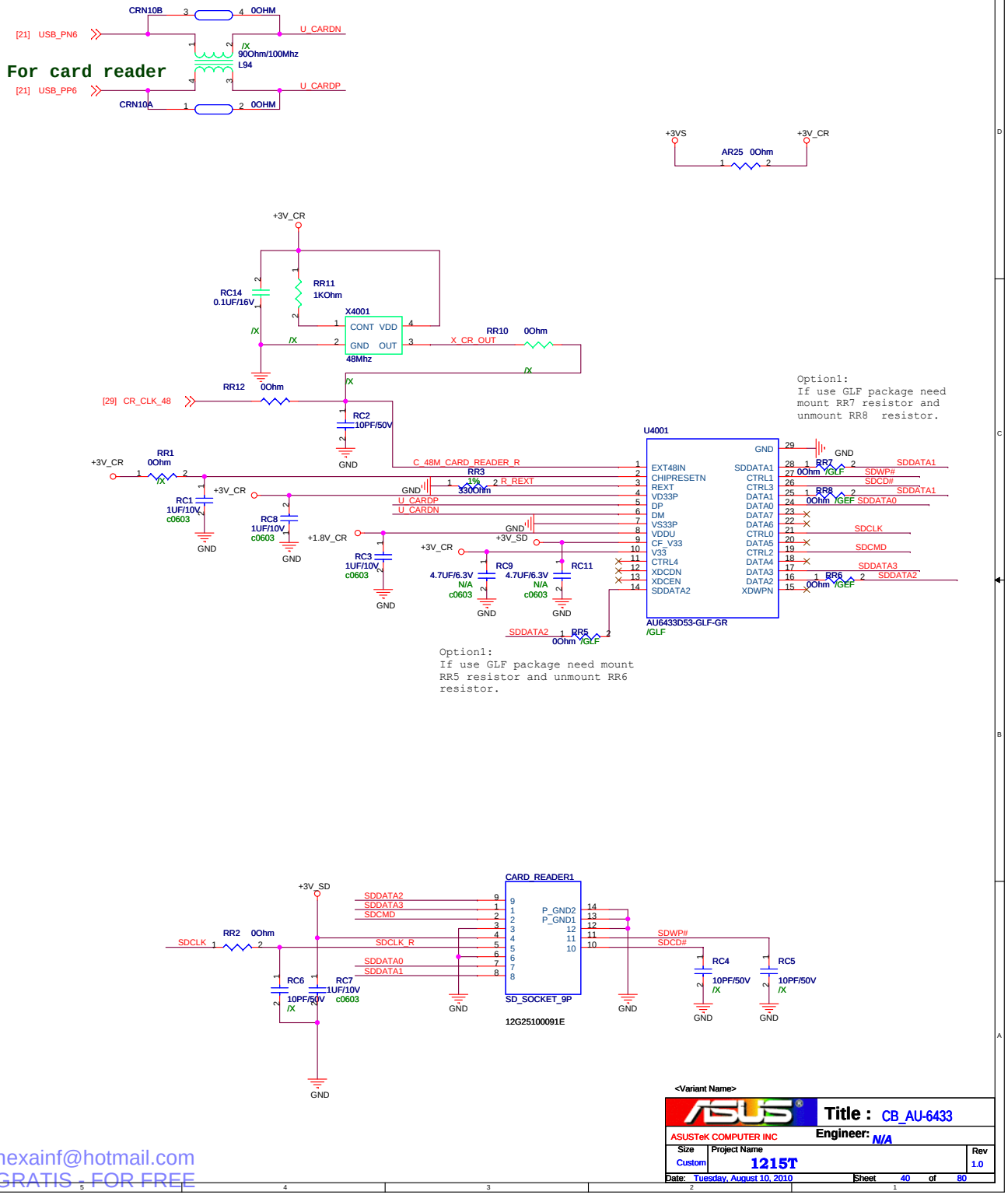

<Variant Name>

Title : CB_AU-6433

ASUSTeK COMPUTER INC

Engineer: N/A

Size	Project Name	Rev
Custom	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 40 of 80

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<variant_name><Variant Name></variant_name>

3.5G Module & External Antenna

Title :

ASUSTek Computer INC.

Engineer: N/A

Size	Project Name	Rev
Custom	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 41 of 80

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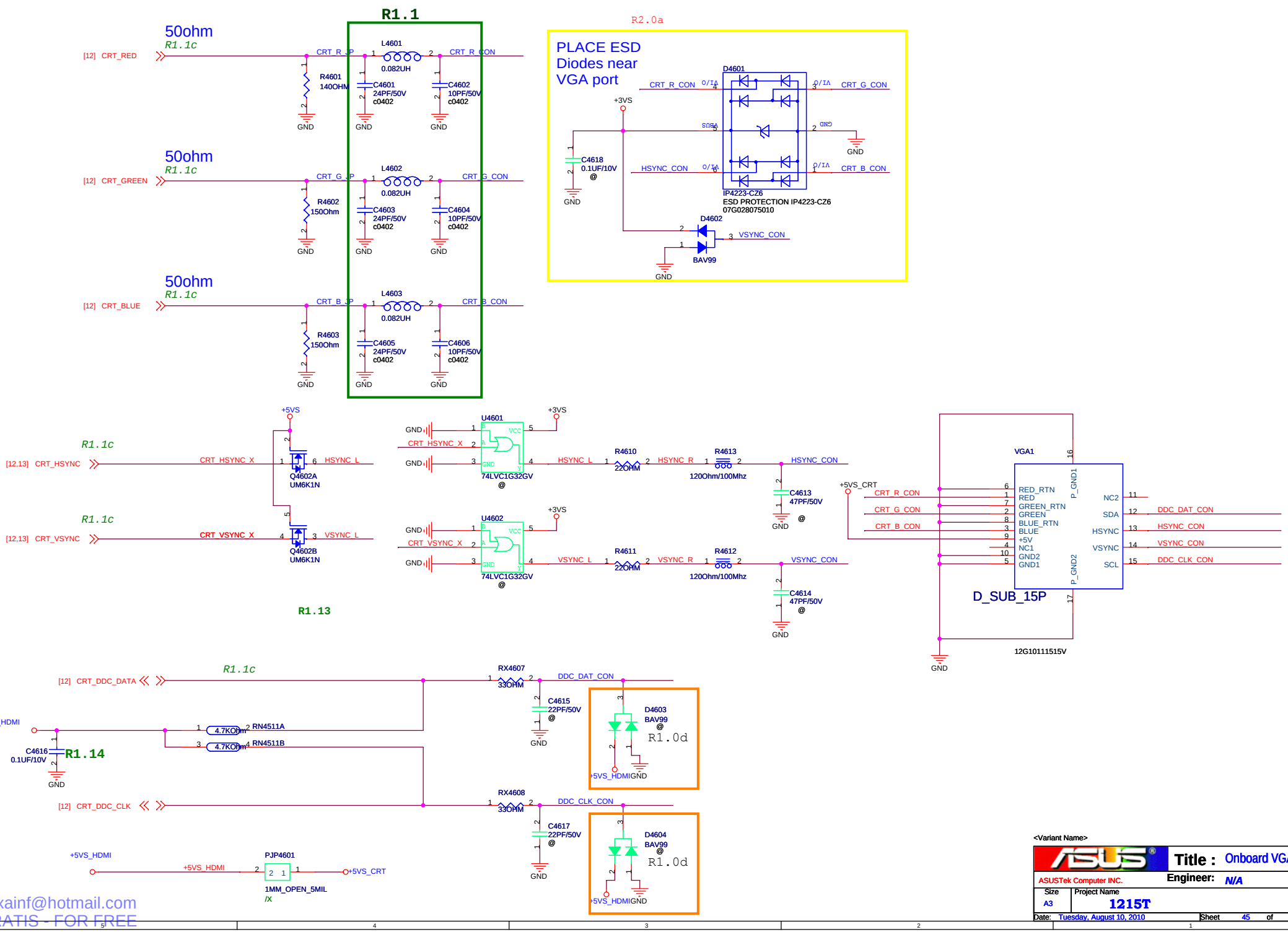


<Variant Name>

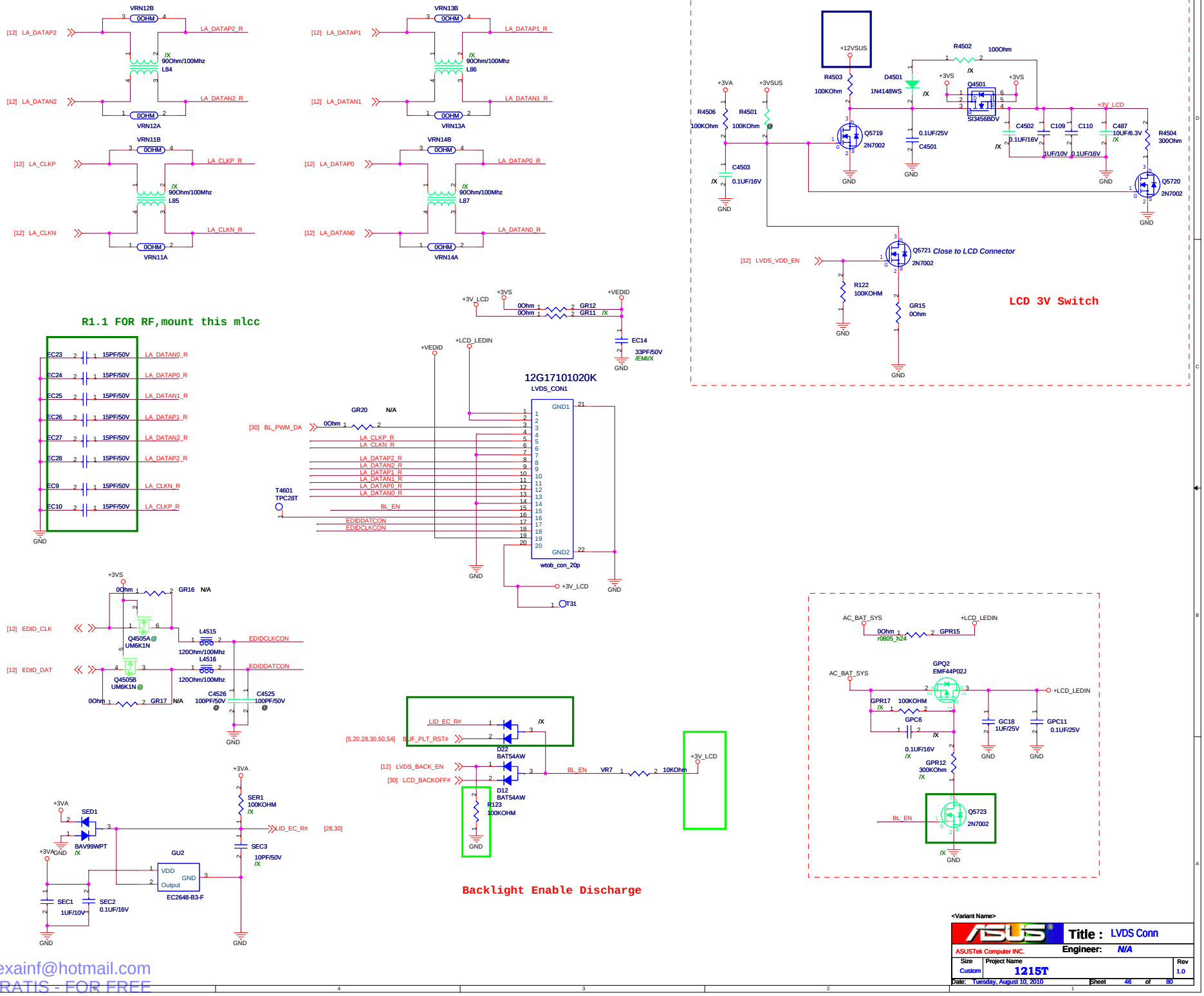
ASUSTek Computer INC.

Title : Onboard VGA

Engineer: N/A

Size	Project Name	Rev
A3	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 45 of 80

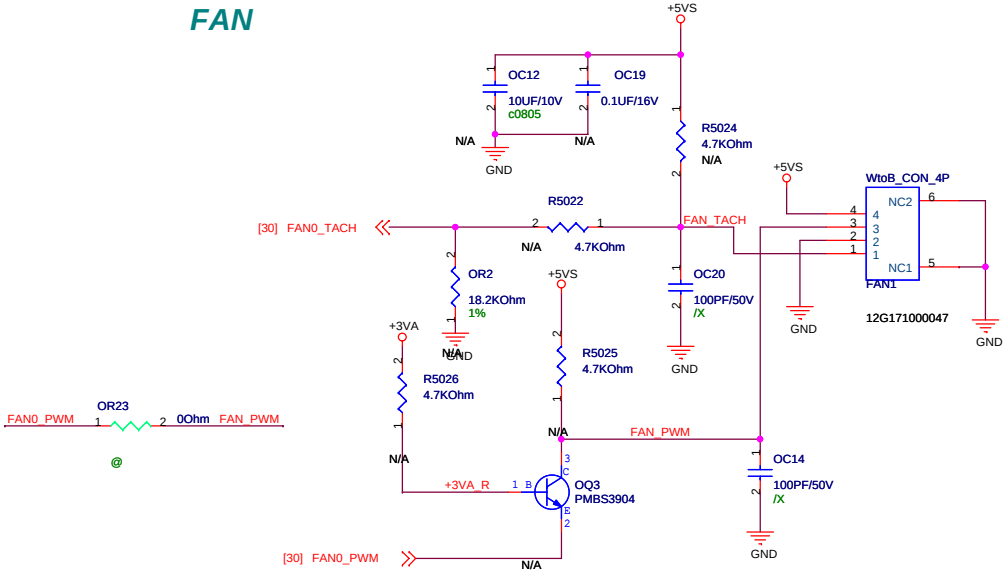


hexainf@hotmail.com
GRATIS - FOR FREE

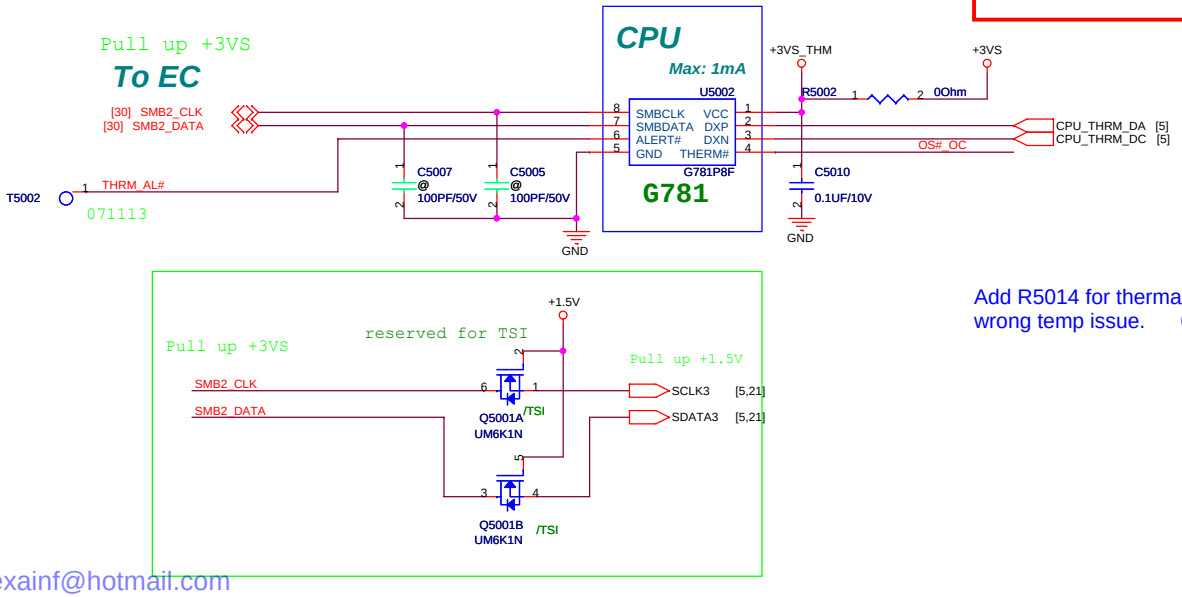
<Variant Name>

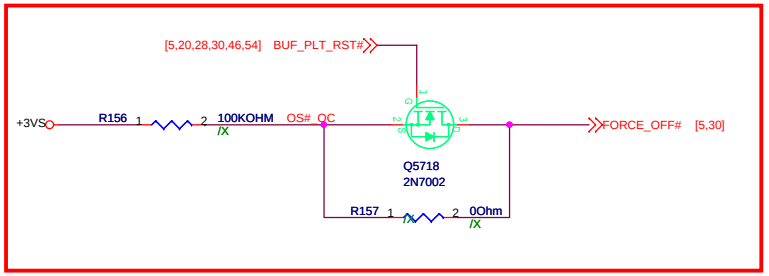
ASUSTek Computer INC.	Title : LVDS Conn	
	Engineer: N/A	
Size: Custom	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 46 of 80	

FAN



Thermal Sensor





<Variant Name>

ASUSTek Computer INC.	Title : FAN_THERMAL SENSOR	
	Engineer: N/A	
Size: Custom	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 50 of 80	

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GRATIS - FOR FREE

<Variant Name>

ASUSTek Computer INC.	Title : USB3.0 Fresco	
	Engineer: N/A	
Size: C	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 51 of 80	

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GRATIS - FOR FREE

Title :	USB 3.0_PORT
ASUSTeK COMPUTER INC. NB4	Engineer: NA
Size: Custom	Project Name: 1215T
Rev: 1.0	
Date: Tuesday, August 10, 2010	Sheet 52 of 80

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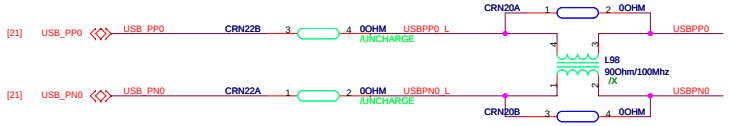
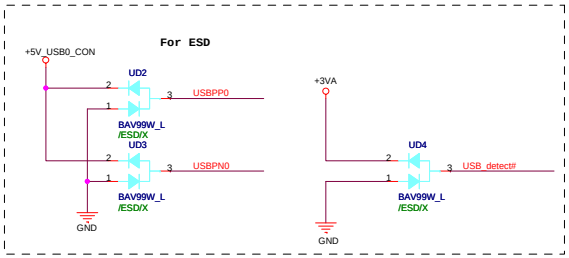
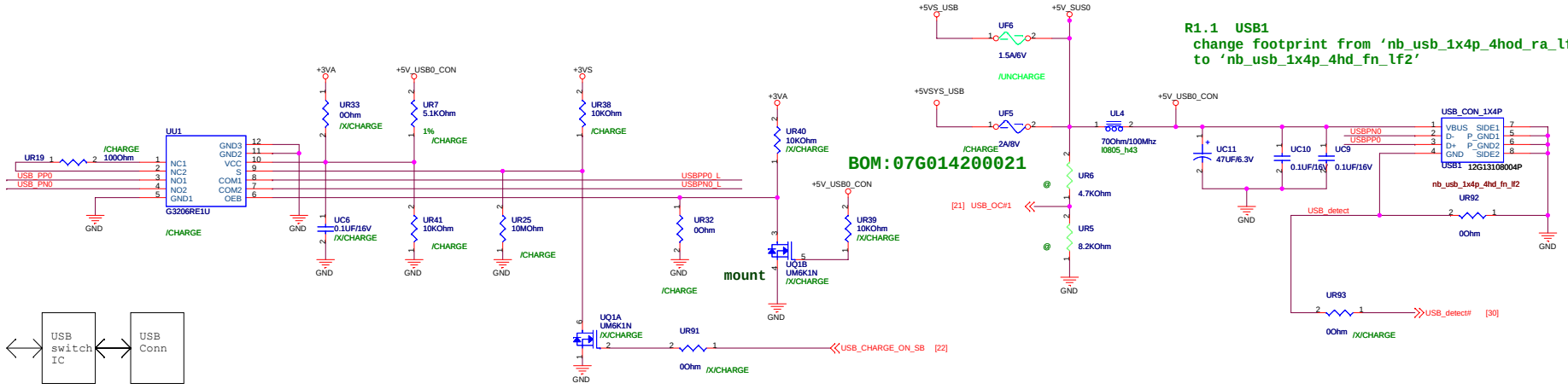
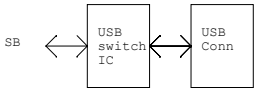
USB2.0 with charge Connector(Optional)









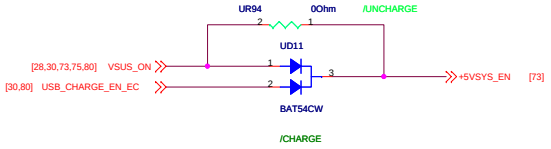
BOM:07G014200021

mount UQ1 in the BOM

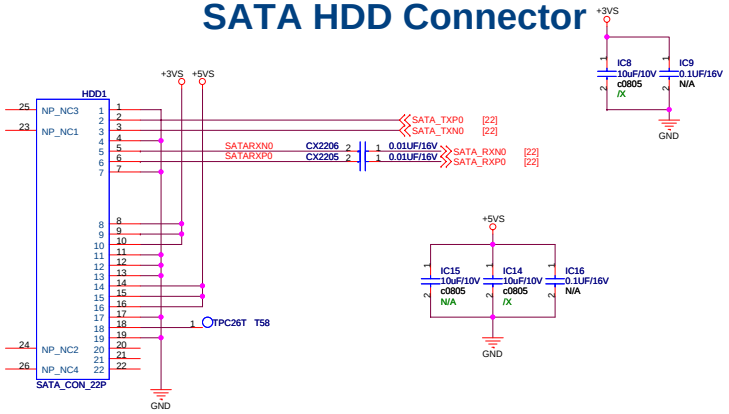
R1.1 USB1
change footprint from 'nb_usb_1x4p_4hod_ra_lf2'
to 'nb_usb_1x4p_4hd_fn_lf2'

Function Table

S	OEB	FUNCTION
X	H	Switch Disconnected
L	L	NC connected to Com
H	L	NO connected to Com



SATA HDD Connector



USB2.0 Connector

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GRATIS - FOR FREE

<Variant Name>

Title : USB Port
ASUSTek Computer INC.
Engineer: N/A
Size: C
Project Name: 1215T
Rev: 1.0
Date: Tuesday, August 10, 2010
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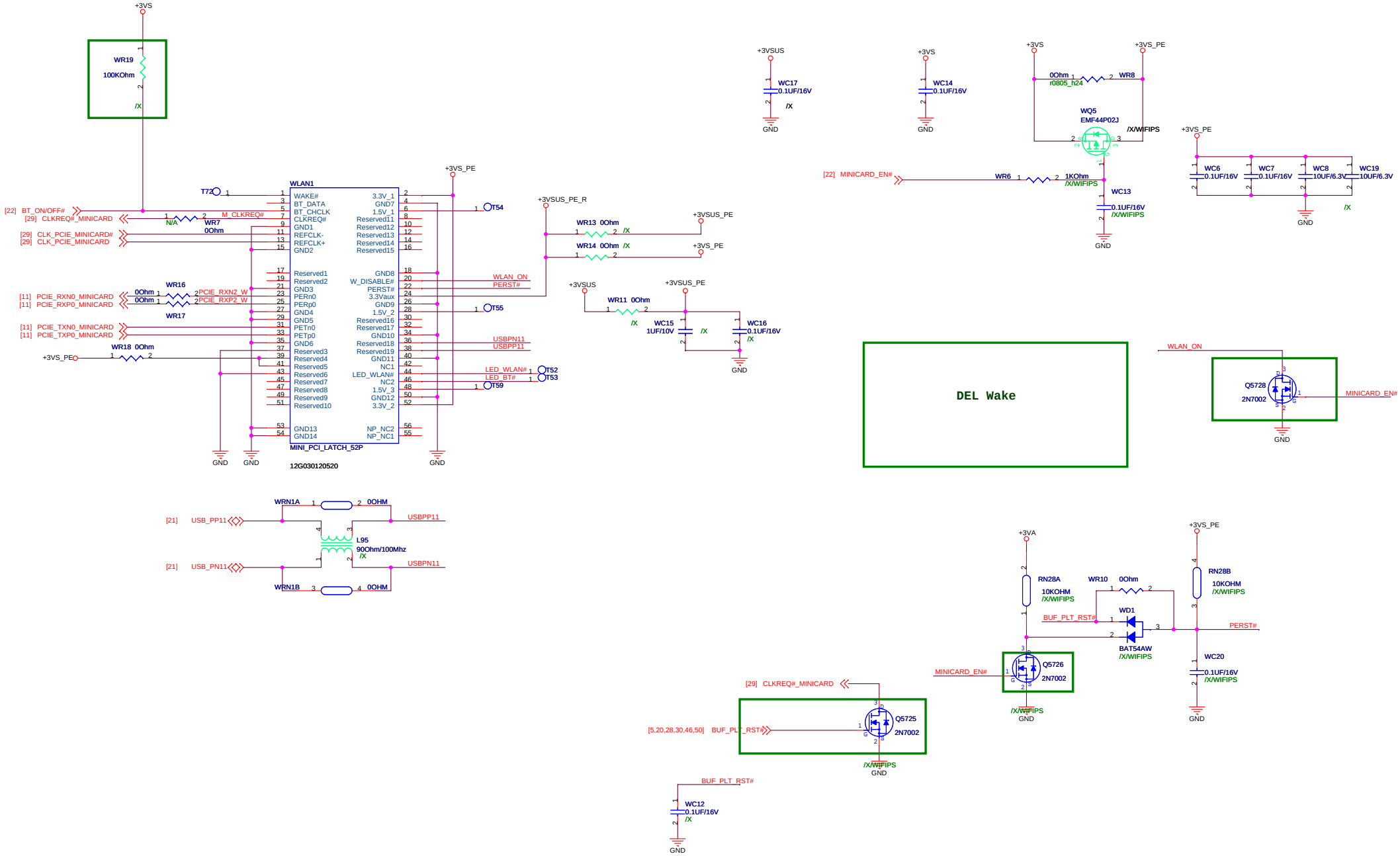

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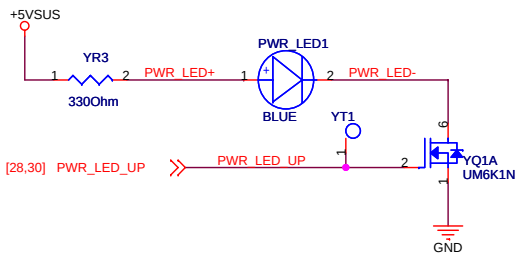
GRATIS - FOR FREE

<Variant Name>

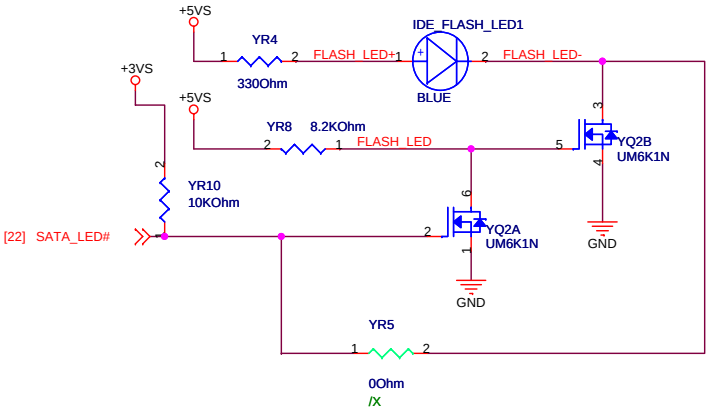
ASUSTek Computer INC.	Title : Mini WIFI	
	Engineer: N/A	
Size: Custom	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 54 of 80	

For POWER LED

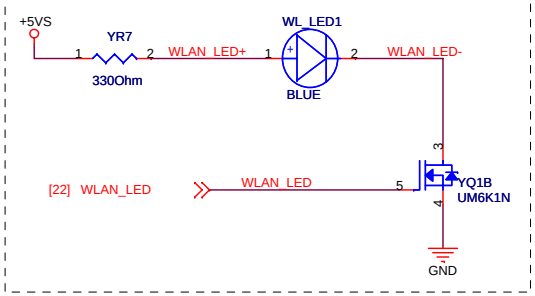


Scenario \ Mode	Adapater Mode	Battery Mode
Battery power is between 100%~40%	Orange ON	Green ON
Battery power is between 40%~10%	Orange Blinking Slowly	Green Blinking Slowly
Battery power is less than 10%	Orange Blinking Quickly	OFF
S3/S5 Mode	Scenario the same as above	

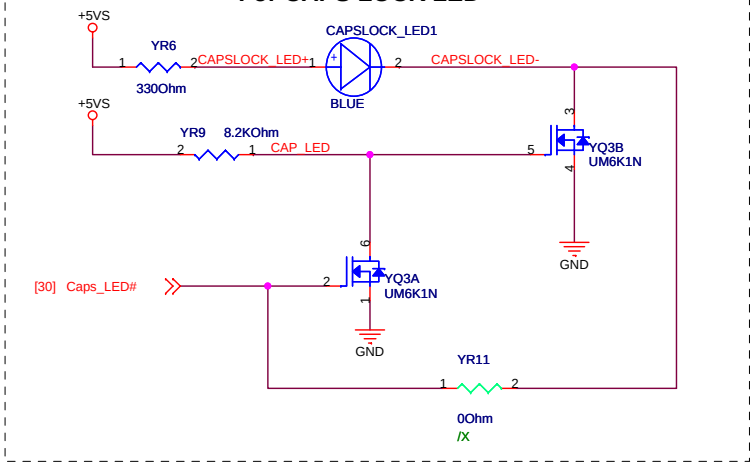
For IDE/SATA LED



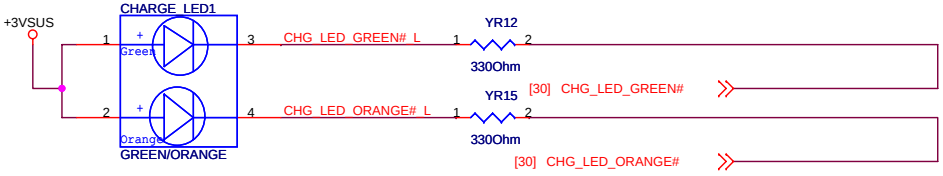
For WLAN LED



For CAPS LOCK LED



For CHARGE LED



<Variant Name>

ASUSTeK COMPUTER INC

Title : LED/PWR SWICH

Engineer: NA

Size	Project Name	Rev
B	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 56 of 80

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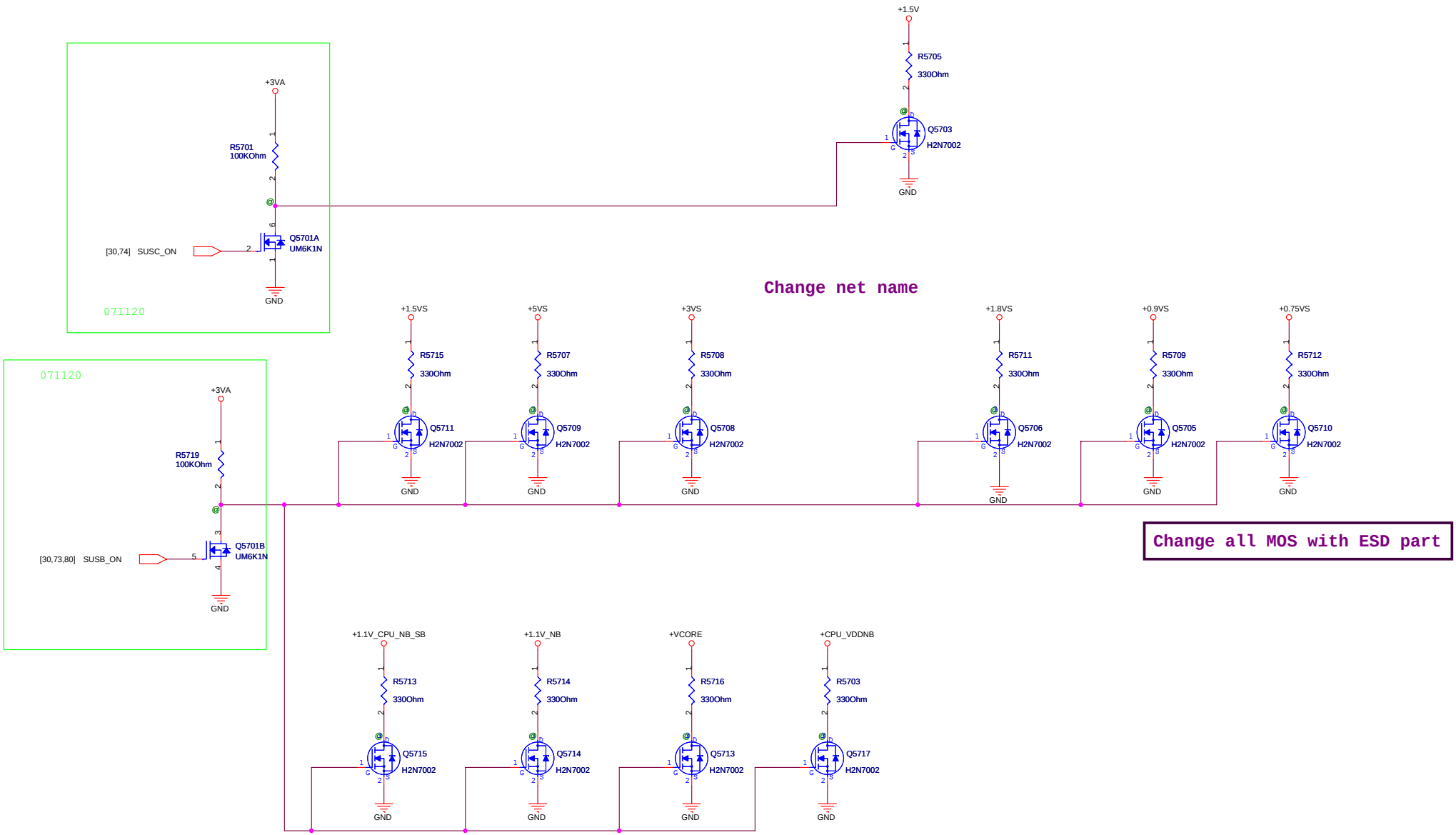

<Variant Name>

ASUSTeK COMPUTER INC

Title : DISCHARGE CKT

Engineer: N/A

Size	Project Name	Rev
Custom	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 57 of 80

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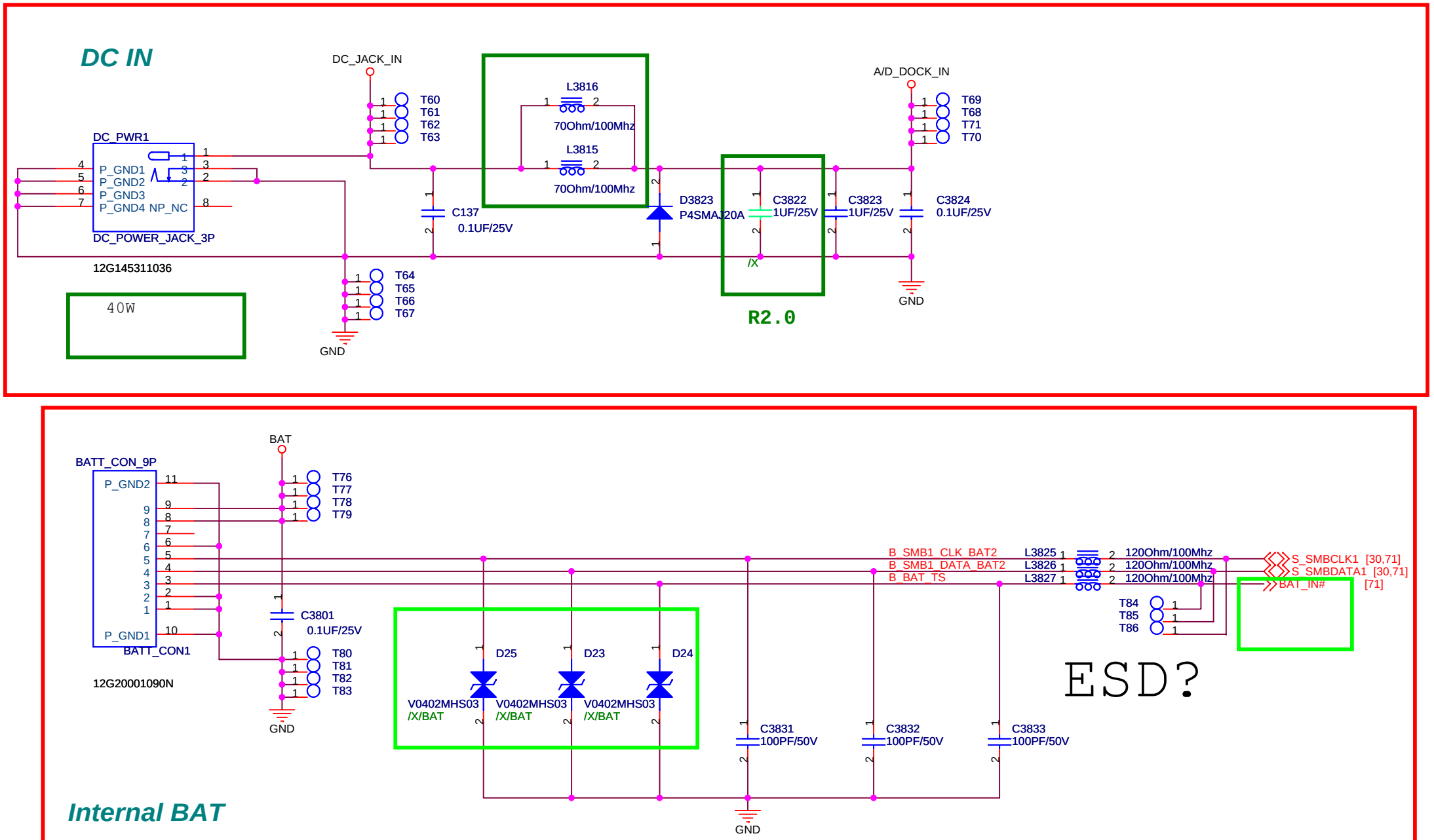
GRATIS - FOR FREE



<Variant Name>

ASUSTek Computer INC.	Title : PWR Jack	
	Engineer: N/A	
Size: A4	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 60 of 80	

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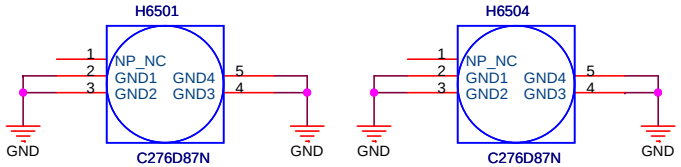
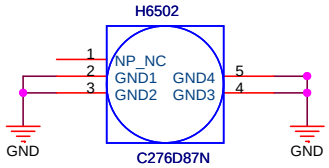
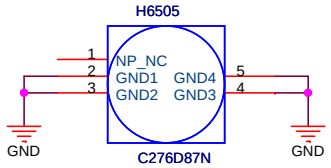
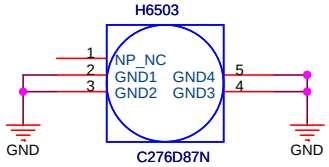
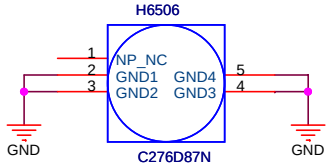
GRATIS - FOR FREE

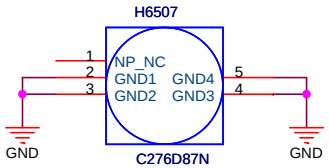




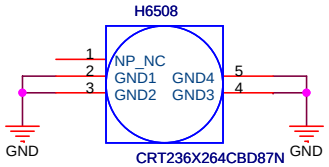


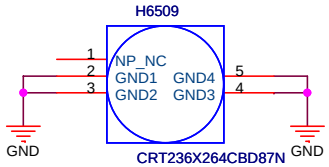




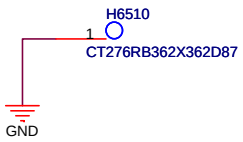


TYPE A SCREW HOLE

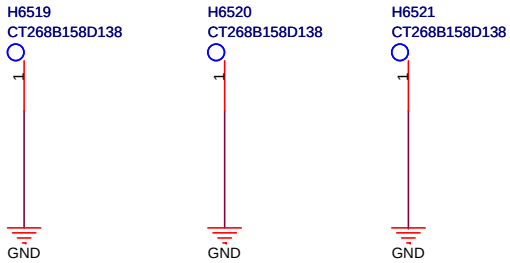




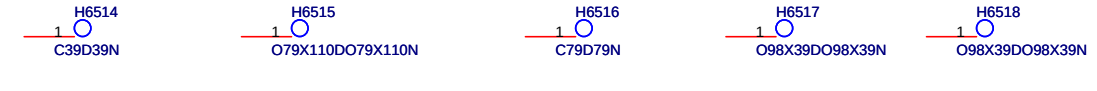
TYPE B SCREW HOLE



TYPE C SCREW HOLE



CPU Braket Hole



1mm E hole **2x2.8mm C hole** **2mm B hole** **2.5x1mm A hole** **2.5x1mm A hole**

HOLE

NUT

<Variant Name>

ASUSTek Computer INC.	Title : Screw Hole	
	Engineer: N/A	
Size: Custom	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 65 of 80	

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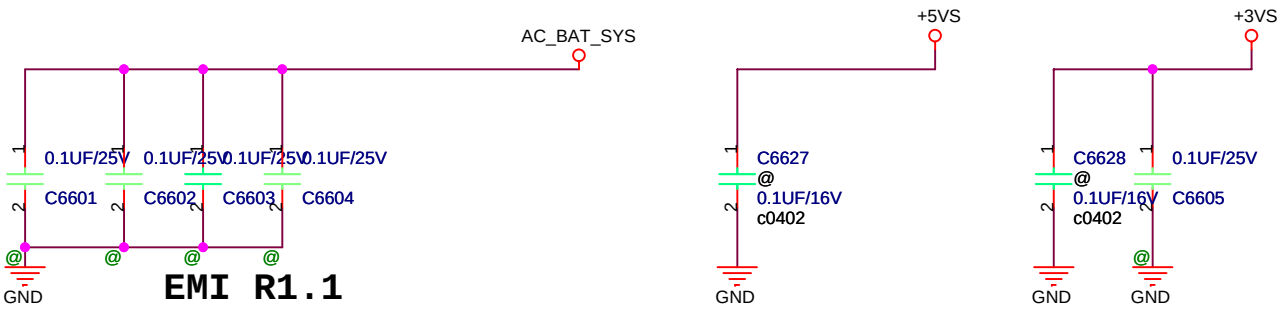
GRATIS - FOR FREE



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GRATIS - FOR FREE

<Variant Name>

ASUSTeK COMPUTER INC

Title : EMI

Engineer: N/A

Size	Project Name	Rev
Custom	1215T	1.0

Date: Tuesday, August 10, 2010 Sheet 66 of 80

ADD

0518：
add EMI Cap;
add R4806/R4807/Q4804

0520：
addT4601/PR167

DELETE

0520：
DEL PC85 PR107 PR12 PR87

MODIFY

0517:
switch TP button PIN1 to PIN3;PIN2 to PIN4

<Variant Name>

ASUSTek Computer INC.	Title : History	
	Engineer: N/A	
Size: B	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 68 of 80	

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<Variant Name>

ASUSTek Computer INC.	Title : Small borad	
	Engineer: N/A	
Size: C	Project Name: 1215T	Rev: 1.0
Date: Tuesday, August 10, 2010	Sheet 69 of 80	

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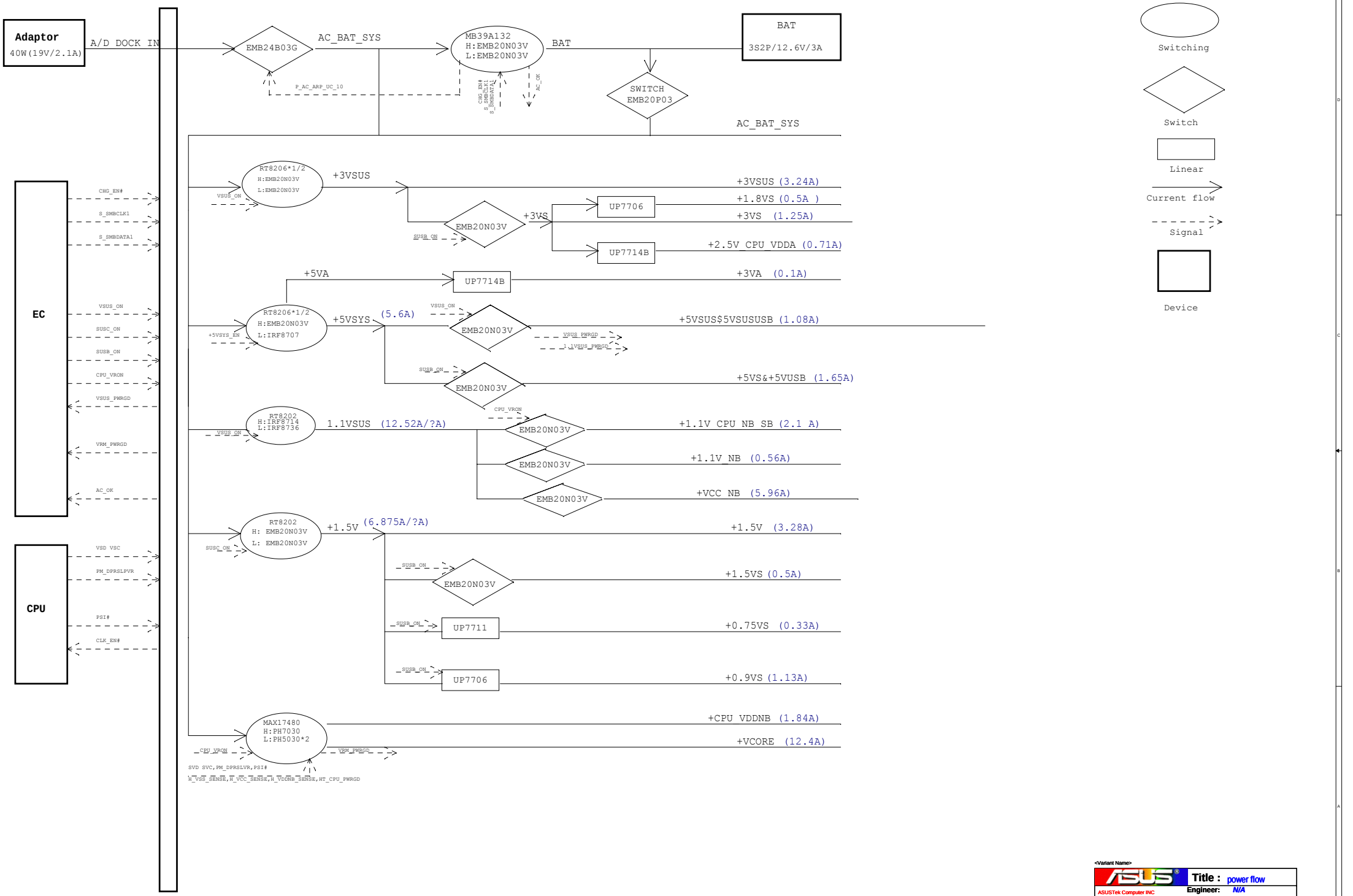

<Variant Name>

ASUSTek Computer INC

Title : power flow

Engineer: N/A

Size	Project Name	Rev
A2	1015T	1.0

Date: Tuesday, August 10, 2010 Sheet 70 of 80

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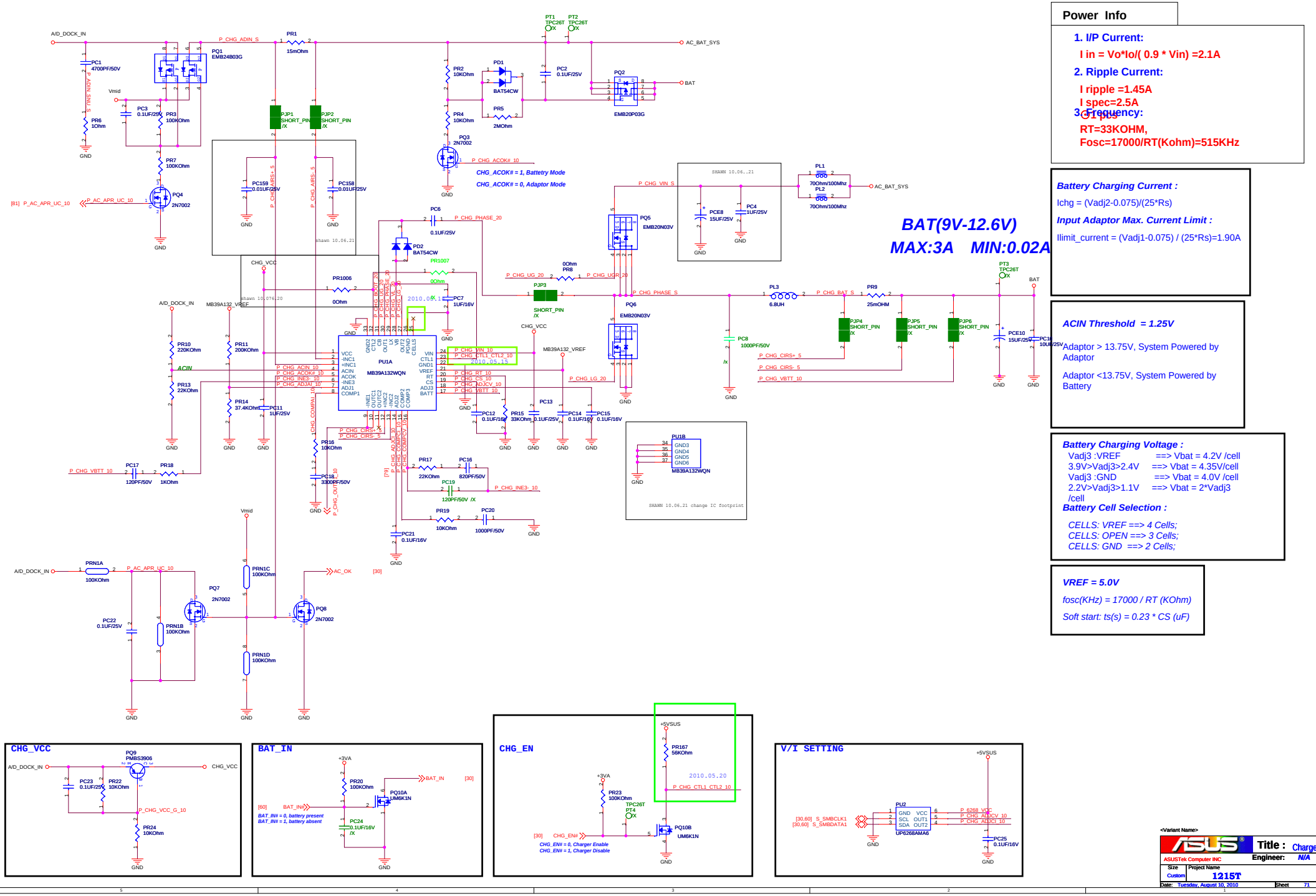
GRATIS - FOR FREE



Power Info

1. I/P Current:
   I in = Vo*Io/(0.9 * Vin) =2.1A
2. Ripple Current:
   I ripple =1.45A
   I spec=2.5A
3. Frequency:
   RT=33KOHM,
   Fosc=17000/RT(Kohm)=515KHz

Battery Charging Current :

Ichg = (Vadj2-0.075)/(25*Rs)

Input Adaptor Max. Current Limit :

Ilimit_current = (Vadj1-0.075) / (25*Rs)=1.90A

ACIN Threshold = 1.25V

Adaptor > 13.75V, System Powered by Adaptor

Adaptor <13.75V, System Powered by Battery

Battery Charging Voltage :

Vadj3 :VREF ==> Vbat = 4.2V /cell
3.9V>Vadj3>2.4V ==> Vbat = 4.35V/cell
Vadj3 :GND ==> Vbat = 4.0V /cell
2.2V>Vadj3>1.1V ==> Vbat = 2*Vadj3 /cell

Battery Cell Selection :

CELLS: VREF ==> 4 Cells;
CELLS: OPEN ==> 3 Cells;
CELLS: GND ==> 2 Cells;

VREF = 5.0V

fosc(KHz) = 17000 / RT (KOhm)

*Soft start: ts(s) = 0.23 * CS (uF)*

<Variant Name>

ASUSTek Computer INC

Title : Charger

Engineer: N/A

Size	Project Name	Rev
Custom	1215T	1.1

Date: Tuesday, August 10, 2010 Sheet 71 of 80

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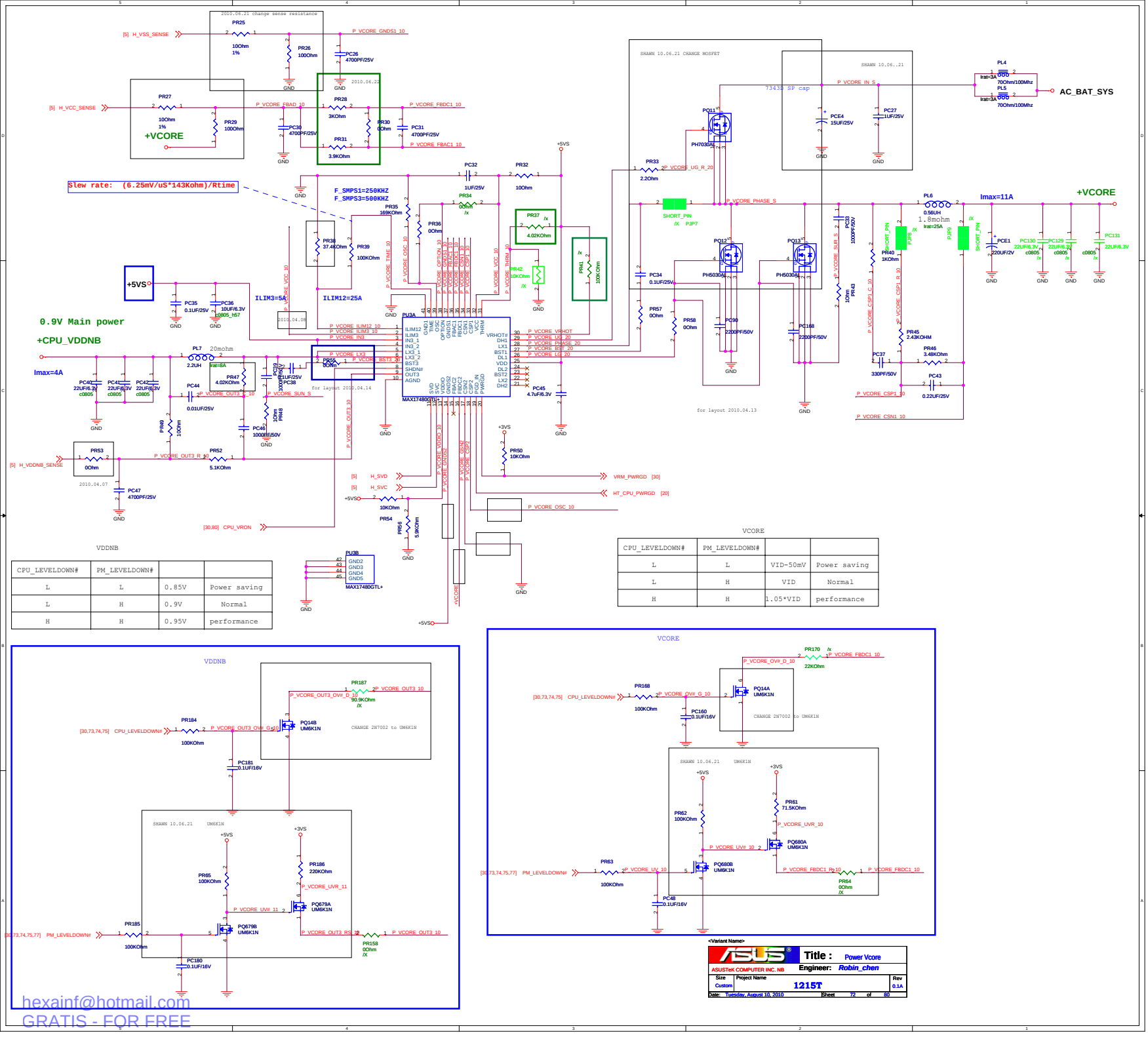
GRATIS - FOR FREE



CPU_LEVELDOWN#	PM_LEVELDOWN#		
L	L	0.85V	Power saving
L	H	0.9V	Normal
H	H	0.95V	performance

VDDNB

CPU_LEVELDOWN#	PM_LEVELDOWN#		
L	L	VID-50mV	Power saving
L	H	VID	Normal
H	H	1.05*VID	performance

VCORE

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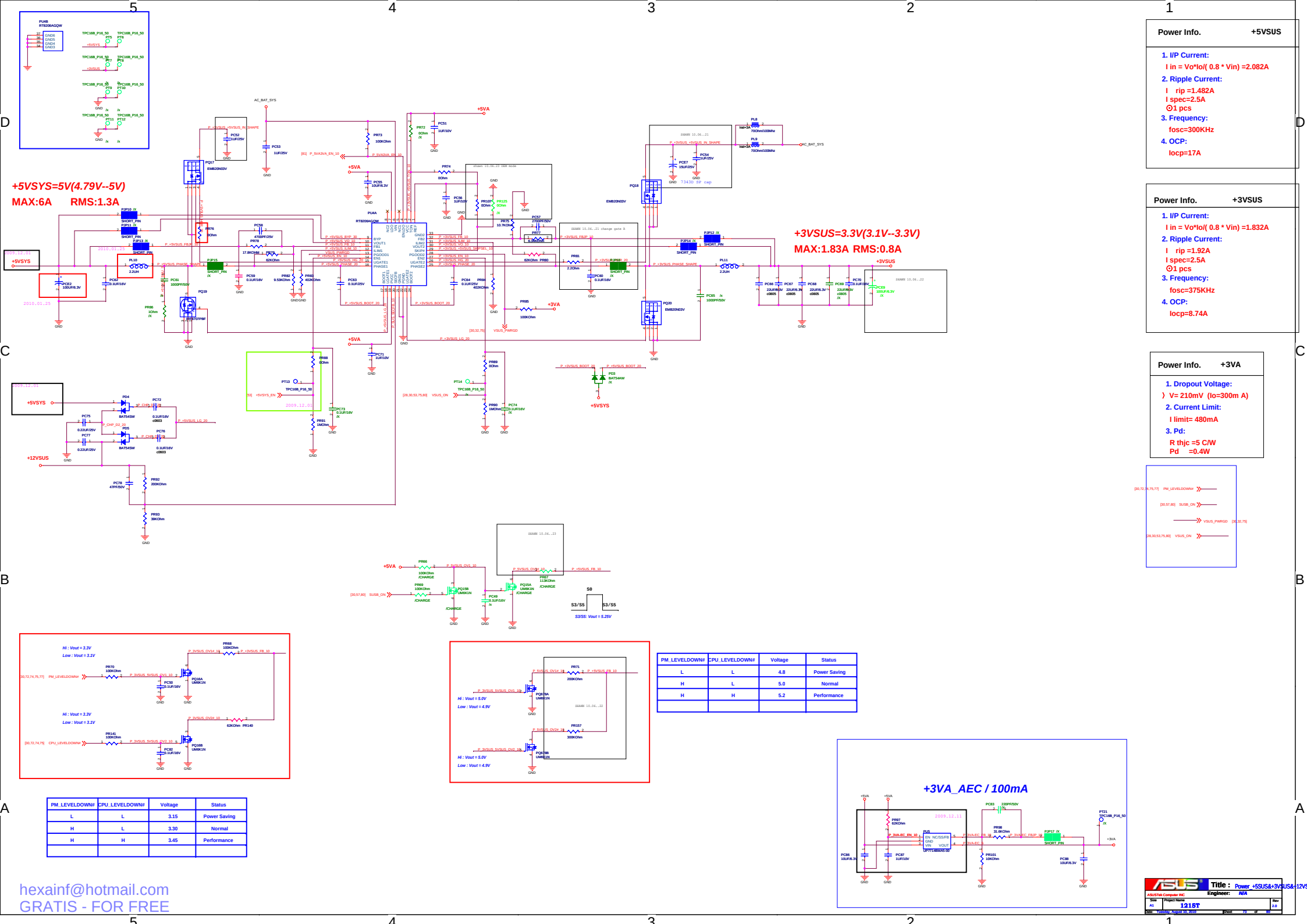


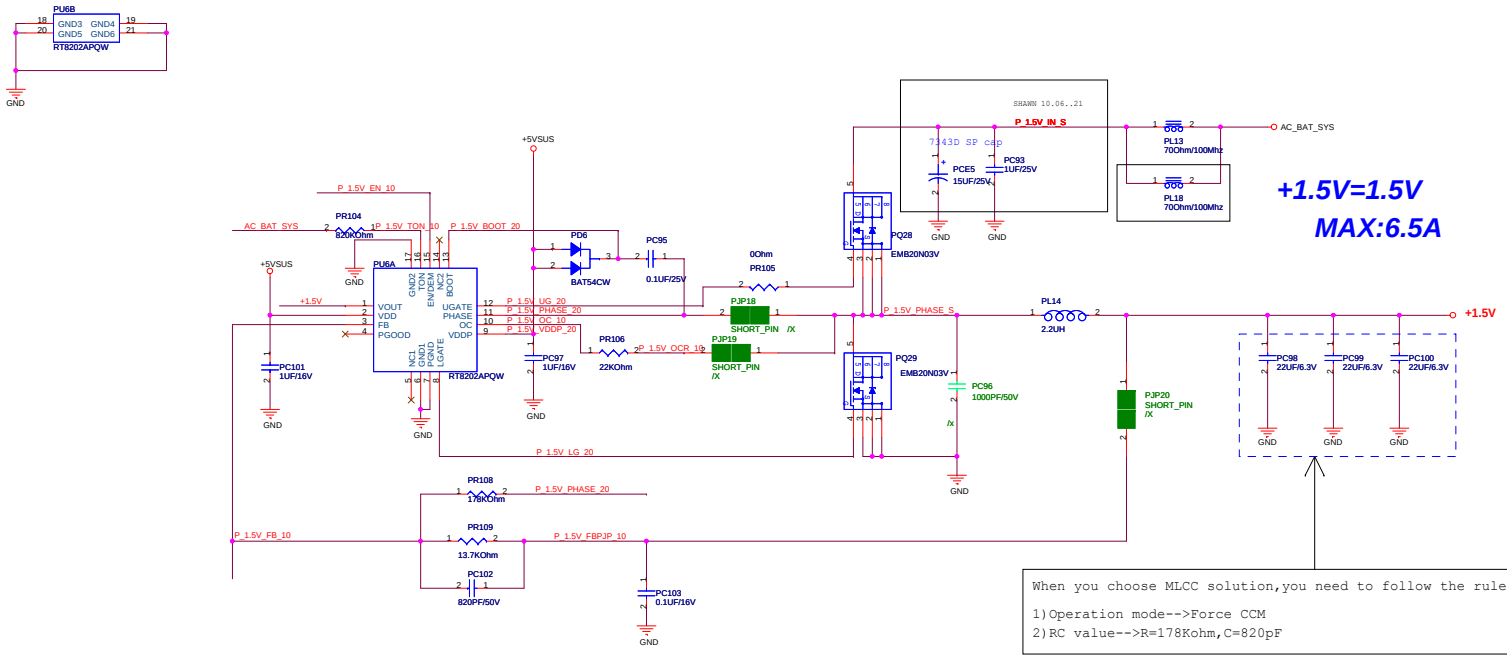
PM_LEVELDOWN#	CPU_LEVELDOWN#	Voltage	Status
L	L	4.8	Power Saving
H	L	5.0	Normal
H	H	5.2	Performance

PM_LEVELDOWN#	CPU_LEVELDOWN#	Voltage	Status
L	L	3.15	Power Saving
H	L	3.30	Normal
H	H	3.45	Performance

Power Info.

1. I/P Current:
   I in = Vo*Io/(0.8 * Vin) =0.825A
2. Ripple Current:
   I rip =1.32A
   I spec=2.5A *
3. Dynamic:
   I peak=3.3A
   ESR=18 mohm
   〉V =59.4mV
4. Frequence
   Fosc=300KHz
5. OCP:
   6.45A

+1.5V=1.5V
MAX:6.5A

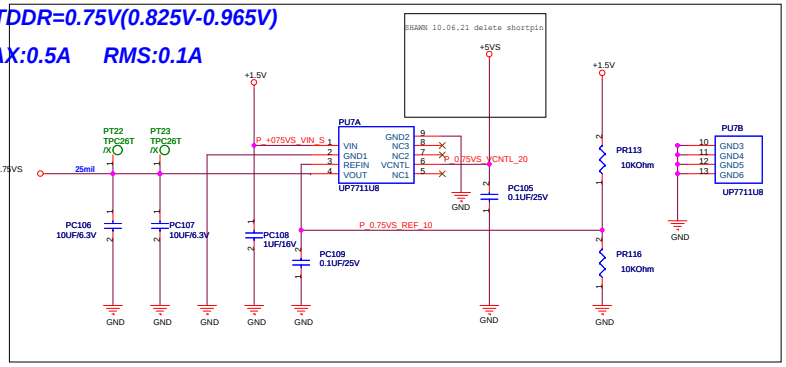


When you choose MLCC solution,you need to follow the rule:

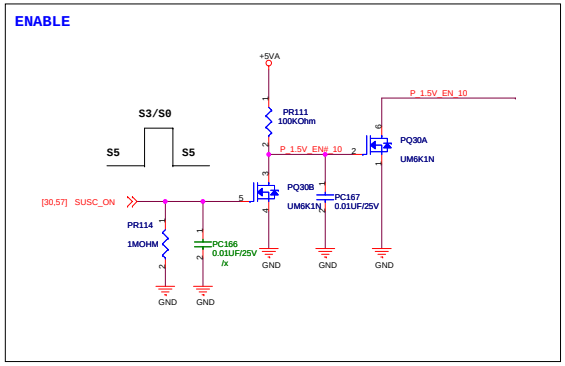
1)Operation mode-->Force CCM
2)RC value-->R=178Kohm,C=820pF

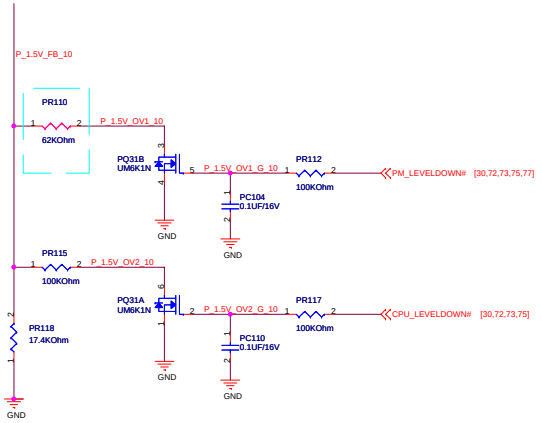
PM_LEVELDOWN#	CPU_LEVELDOWN#	Voltage	Status
L	L	1.4V	Power Saving
H	L	1.5V	Normal
H	H	1.6V	Performance

+VTTDDR=0.75V(0.825V-0.965V)
MAX:0.5A RMS:0.1A



ENABLE





<Variant Name>

Title : +1.8V&VTTDDR
ASUSTek Computer INC
Engineer: N/A
Size: A2 | Project Name: 1215T | Rev: 1.1
Date: Tuesday, August 10, 2010 | Sheet 74 of 80

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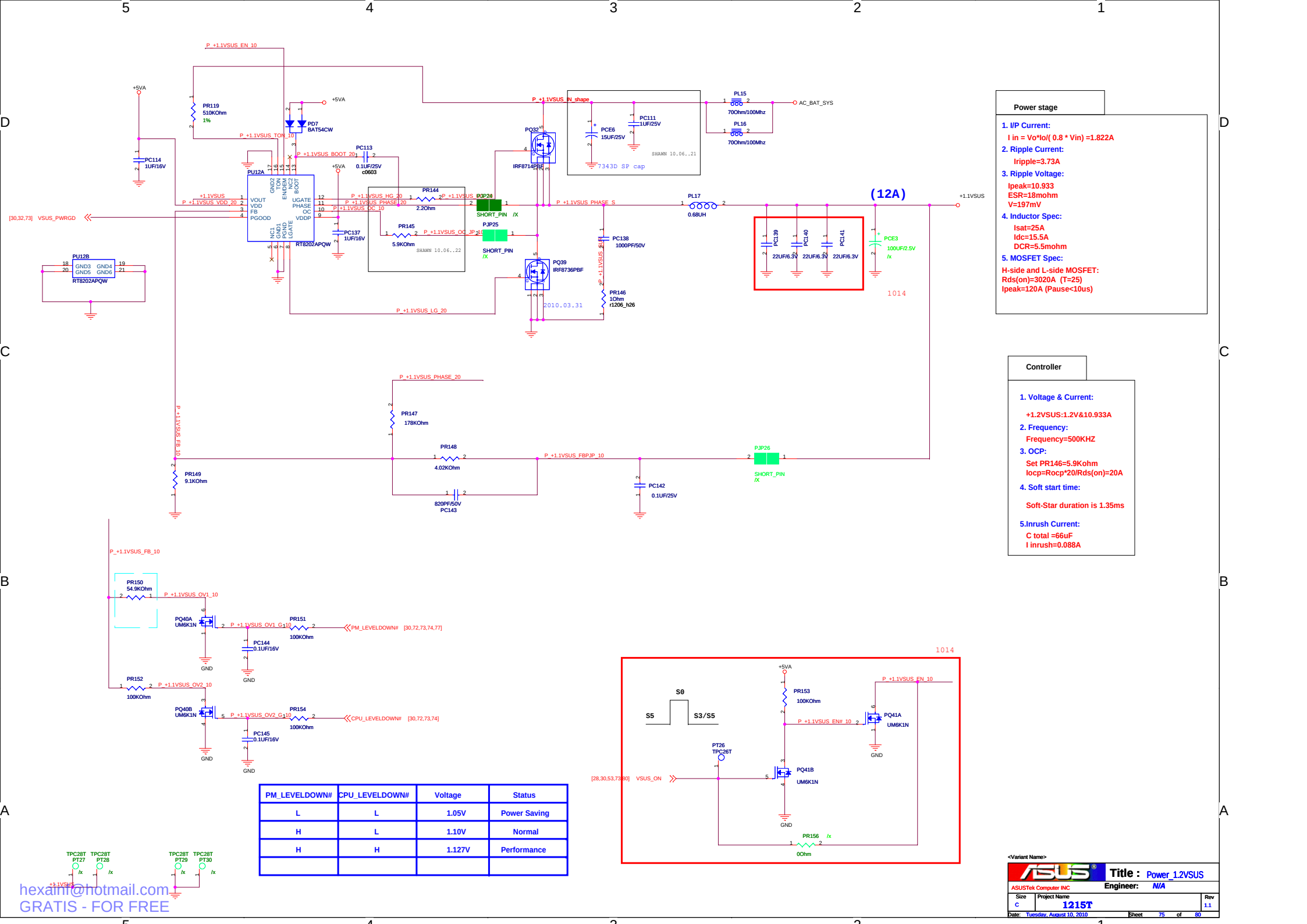

Power stage

1. I/P Current:
   I in = Vo*Io/(0.8 * Vin) =1.822A
2. Ripple Current:
   Iripple=3.73A
3. Ripple Voltage:
   Ipeak=10.933
   ESR=18mohm
   V=197mV
4. Inductor Spec:
   Isat=25A
   Idc=15.5A
   DCR=5.5mohm
5. MOSFET Spec:

H-side and L-side MOSFET:
Rds(on)=3020A (T=25)
Ipeak=120A (Pause<10us)

Controller

1. Voltage & Current:
   +1.2VSUS:1.2V&10.933A
2. Frequency:
   Frequency=500KHZ
3. OCP:
   Set PR146=5.9Kohm
   Iocp=Rocp*20/Rds(on)=20A
4. Soft start time:
   Soft-Star duration is 1.35ms
5. Inrush Current:
   C total =66uF
   I inrush=0.088A

PM_LEVELDOWN#	CPU_LEVELDOWN#	Voltage	Status
L	L	1.05V	Power Saving
H	L	1.10V	Normal
H	H	1.127V	Performance

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<Variant Name>

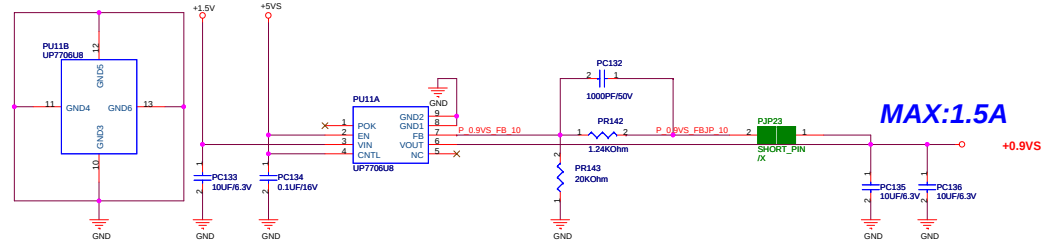
ASUSTek Computer INC

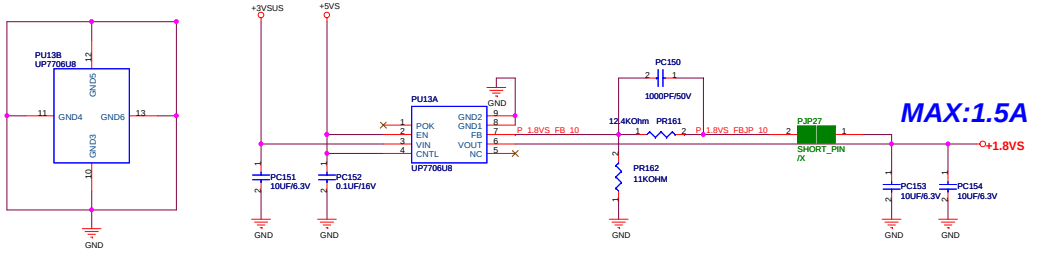
Title : Power_1.2VSUS

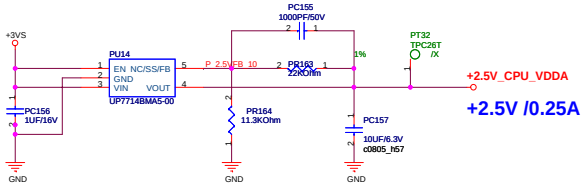
Engineer: N/A

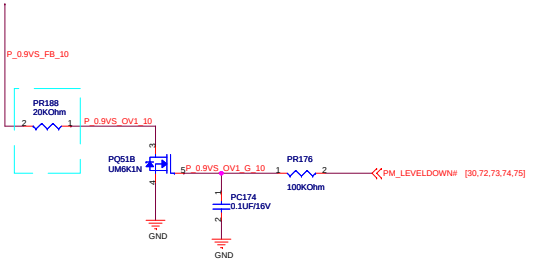
Size	Project Name	Rev
C	1215T	1.1

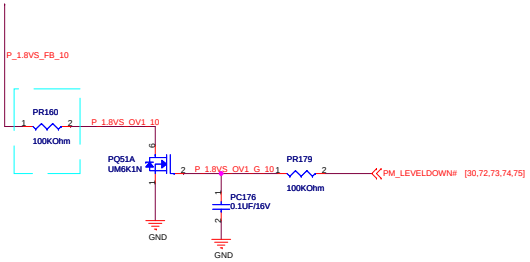
Date: Tuesday, August 10, 2010 Sheet 75 of 80











1. Dropout Voltage:
   〉 V= 300 mV (Io=2 A)
2. Current Limit:
   I limit= 2.8 A
3. Continue Current:
   I cont= 1A
4. Pd:
   R thjc =5 C/W
   Pd =1.9W
5. EN Voltage:
   V rising = 1.4 V
   V falling = 0.4 V
6. Supply Voltage:
   Vcc=5V
7. Inrush current:
   Tss = 4 ms
   C total = 20 uF
   I inrush= 7.5mA

+0.9VS

PM_LEVELDOWN#	CPU_LEVELDOWN#	Voltage	Status
L	L	0.85V	Power Saving
H	L	0.9V	Normal
H	H	0.95V	Performance

+1.8VS

PM_LEVELDOWN#	CPU_LEVELDOWN#	Voltage	Status
L	L	1.7V	Power Saving
H	L	1.8V	Normal
H	H	1.9V	Performance

2.5V @ 0.25A

1. Dropout Voltage:
   〉 V = 0.21V (Io =0.3A)
2. Current Limit:
   I limit =320mA
3. Continue Current:
   I cont = 300mA
4. Power Dissipation:
   Rthjc = 250 /W
   Pd = 0.4W
5. EN Voltage:
   V rising = 2V
   V falling = 0.8V
6. Supply Voltage:
   Vcc =3V
7. Inrush current:
   T ss = 400us
   C total =10uF
   I inrush = 0.063A

<Variant Name>

ASUSTek Computer INC

Title : +1.5VS & +2.5VS

Engineer: N/A

Size	Project Name	Rev
A2	1218T	1.1

Date: Tuesday, August 10, 2010 Sheet 77 of 80

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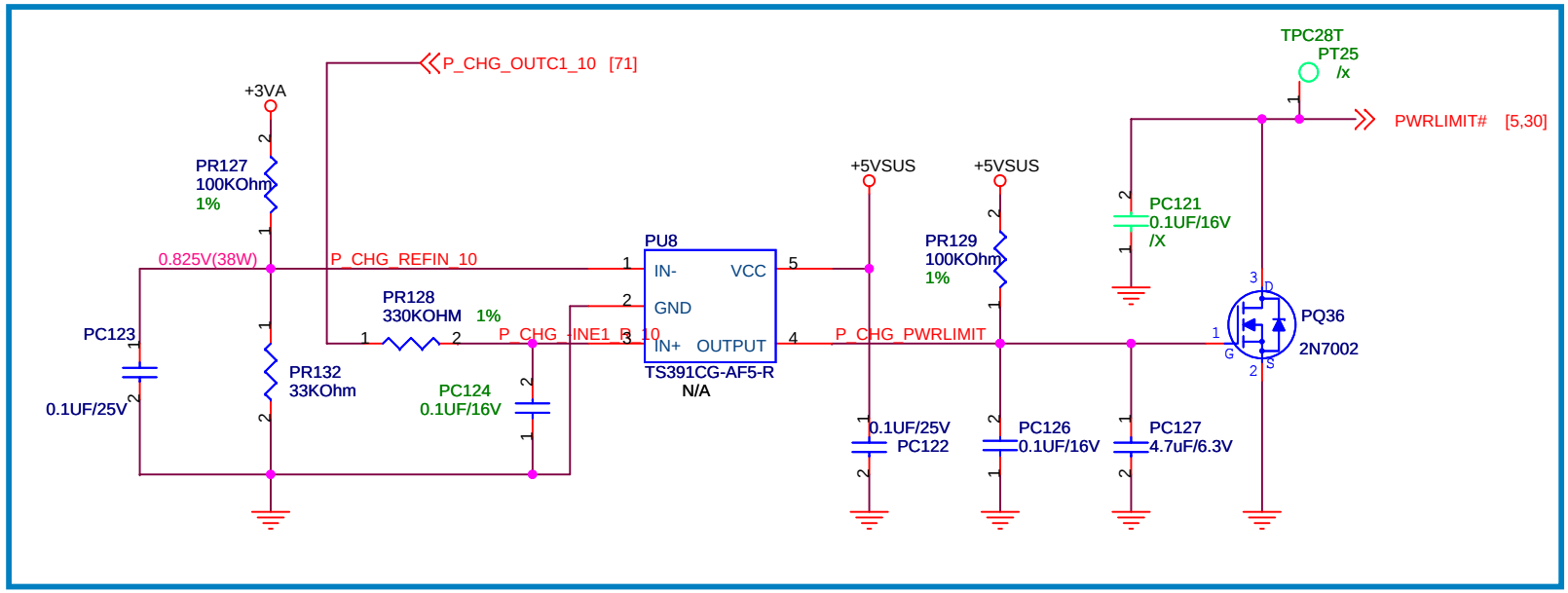

<Variant Name>

ASUSTek Computer INC	Title : Power Lim	
	Engineer: N/A	
Size: A4	Project Name: 1215T	Rev: 1.1
Date: Tuesday, August 10, 2010	Sheet 79 of 80	

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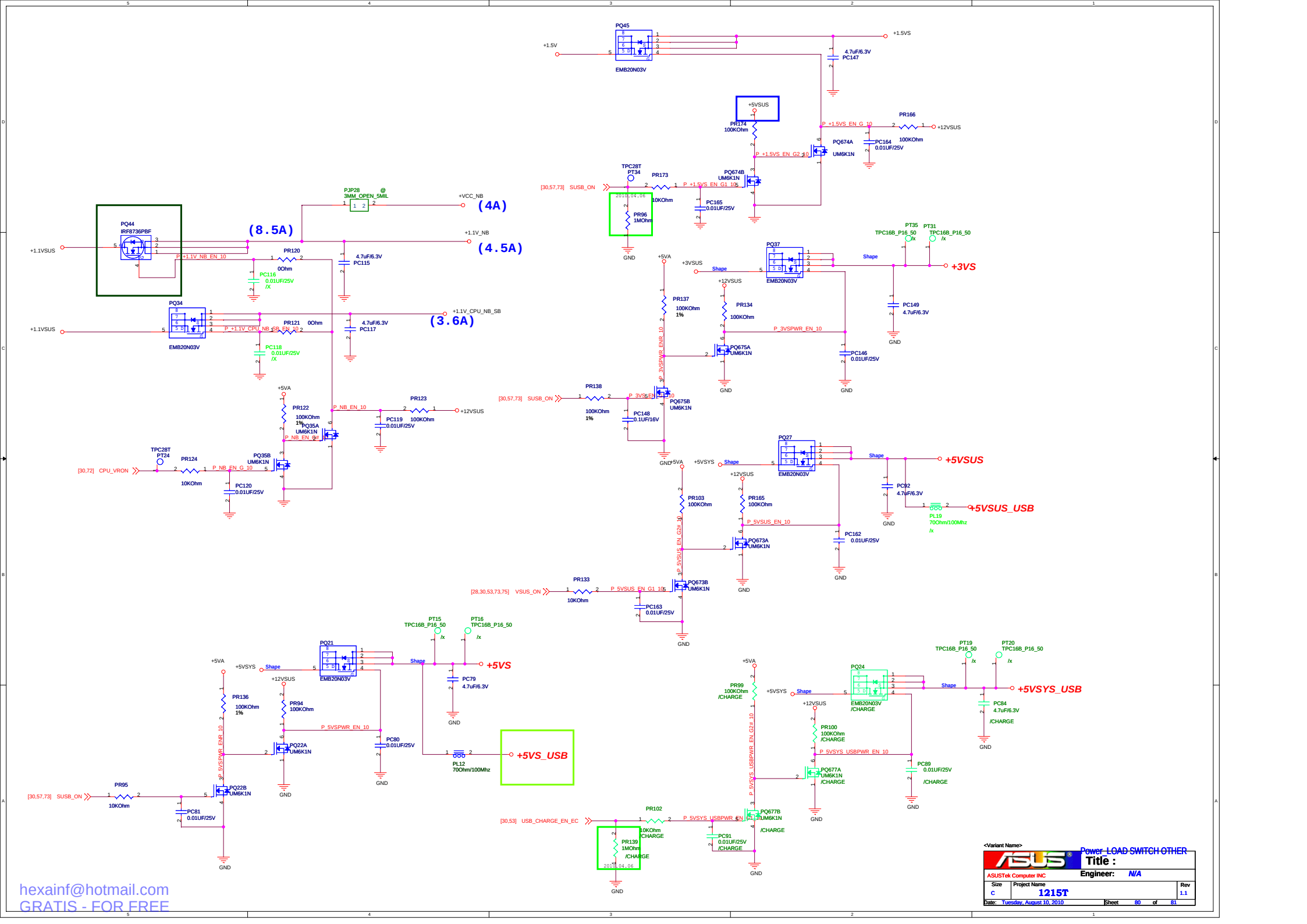

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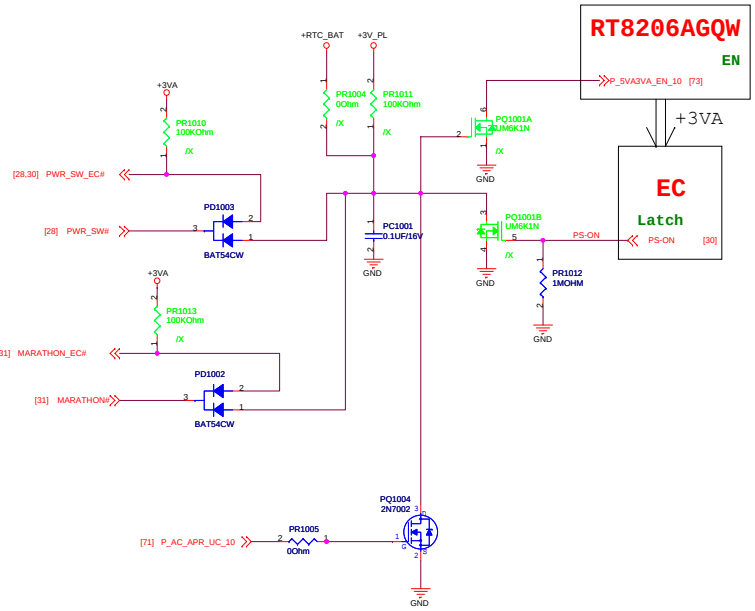
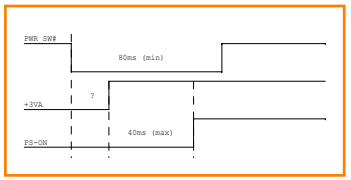
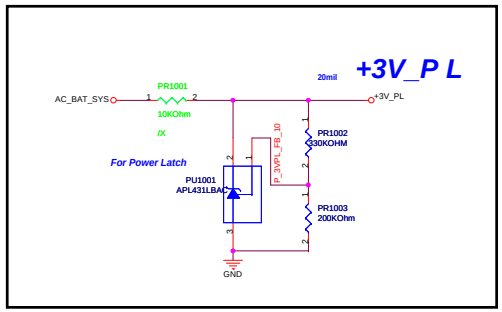
GRATIS - FOR FREE

<variant_name>
Power_LOAD SWITCH OTHER
Title :
ASUSTek Computer INC
Engineer: N/A
Size: C
Project Name: 1215T
Rev: 1.1
Date: Tuesday, August 10, 2010
Sheet 80 of 81
</variant_name>







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GRATIS - FOR FREE

<Variant Name>

ASUSTek Computer INC

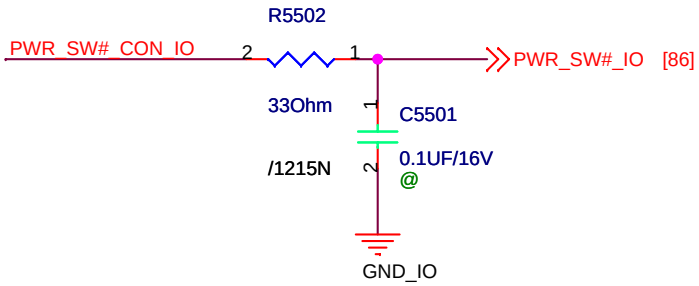
Title : Power Lim

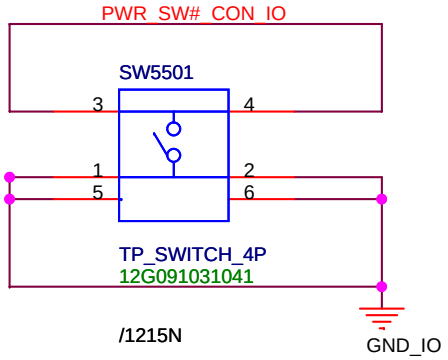
Engineer: N/A

Size	Project Name	Rev
A2	1015T	1.0

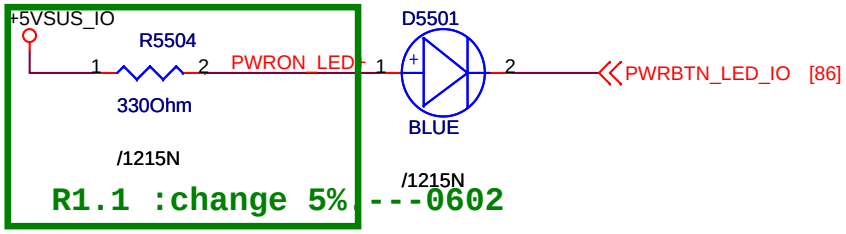
Date: Tuesday, August 10, 2010 Sheet 81 of 82

PWR SW





For POWER ON LED



0521:change +5V_USB_IO to +5VSUS_IO

ASUSTEK COMPUTER INC	Title : PWR_BUTTON_LED	
	Engineer: Anndy_wang	
Size: A	Project Name: 1215N_IO	Rev: 1.3
Date: Tuesday, August 10, 2010	Sheet 82 of 92	

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R1.7 ALC269-VB2 Issue
PD# is internal pull-up to 5VS_AUDIO & VIH=3.3V
Add R3602 &R3613 of PD# to make sure the PD# is higher than 3.3V when power up speaker amplifier

269VA USE 0 ohm/0603

DLY_OP_SD# "L" ==> PD# = 0.37V"H" ==> PD# = 3.55V

269_VA 02G611005006
269_VB 02G611005010
269_VB5 02G611005015

5/26

6/29 DesignIP R1.3

UP7714BMT5-00 (P/N:06G029330020)
Vout=0.8*(1+(49.9K/10K))
=4.792V

EMI 07/03

Place R3606 near U3602

GND
GND_AUDIO

Digital

For VIA VT1802P
C3627 C3628 Change to 2.2UF/10V (P/N 11G233322536360)

For VIA VT1802P
R3601 Change to 5.1Kohm (P/N 10G2125101140030)

For VIA VT1802P
C3615 Change to 0.1uF (P/N 11G233310432340)
C3608 may improve the audio performance

RealTek recommend change C3615 from 2.2uF to 1uF
New project Please use the 1uF for VREF_CODEC
On going project Please keep 2.2uF for VREF_CODEC if speaker have not S3 S4 resume issue.

R1.5 Co-lay for 269_VB

For EMI
EMI 05/26

EMI 05/26

06/19 remove PC beep

For VIA VT1802P
Please reserve 11G232022004320 for ACZ_BCLK_AUD at PCH (SB) side

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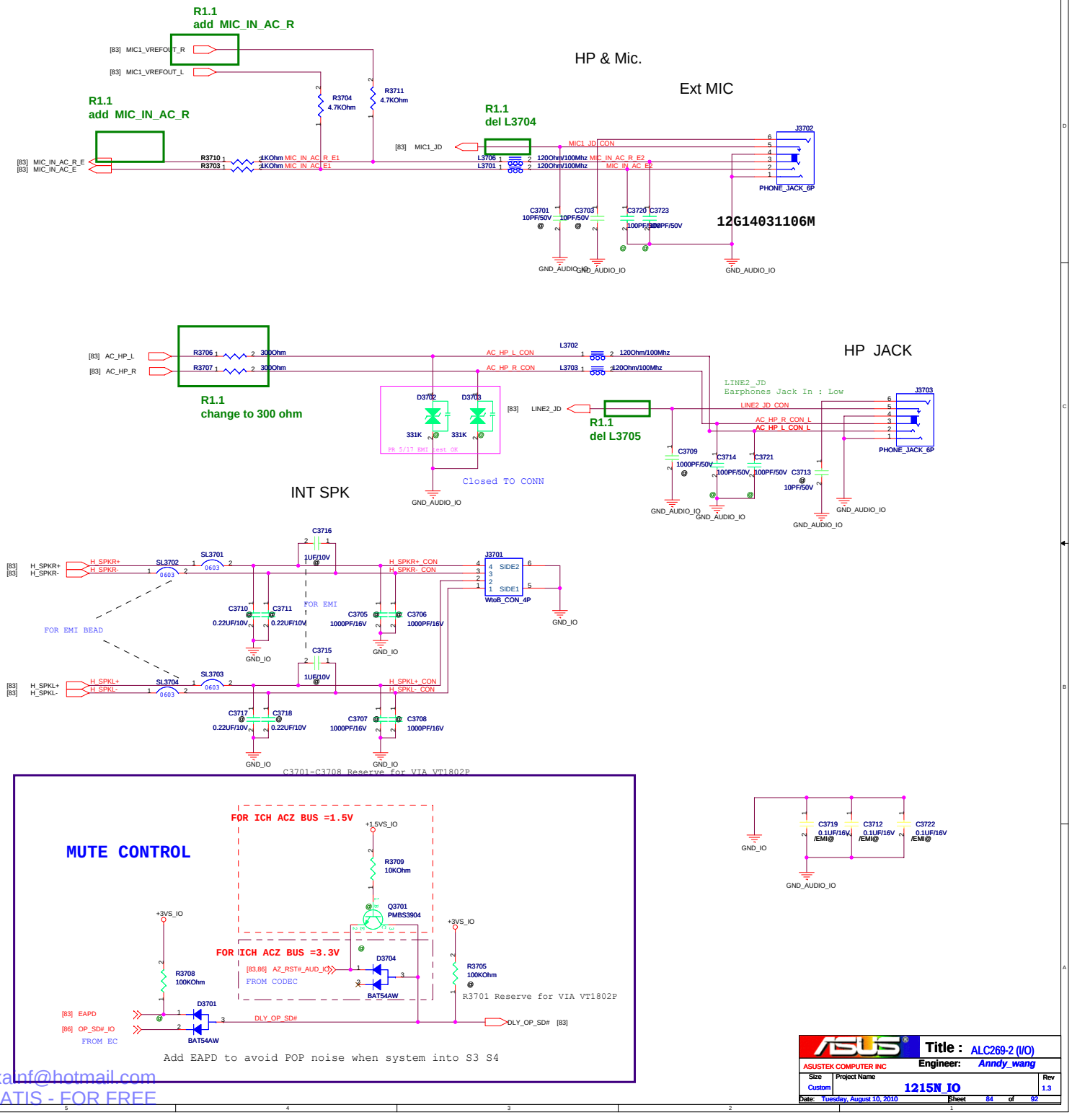
GRATIS - FOR FREE

<Variant Name>

Title : ALC269-1
ASUSTEK COMPUTER INC Engineer: Anndy_wang
Size C | Project Name 1215N_IO | Rev 1.3
Date: Tuesday, August 10, 2010 | Sheet 83 of 92



ASUSTEK COMPUTER INC	Title : ALC269-2 (I/O)		
	Engineer: Anndy_wang		
Size: Custom	Project Name: 1215N_IO		Rev: 1.3
Date: Tuesday, August 10, 2010	Sheet 84 of 92		

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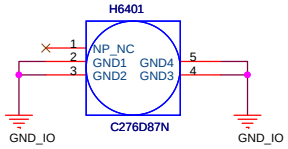
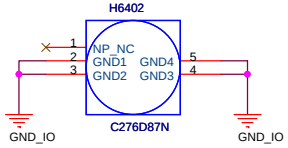
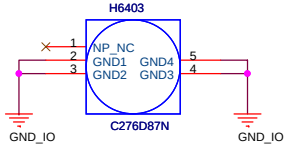
GRATIS - FOR FREE







ASUSTEK COMPUTER INC	Title : Srew Hole	
	Engineer: Anndy_wang	
Size: A3	Project Name: 1215N_IO	Rev: 1.3
Date: Tuesday, August 10, 2010	Sheet 85 of 92	

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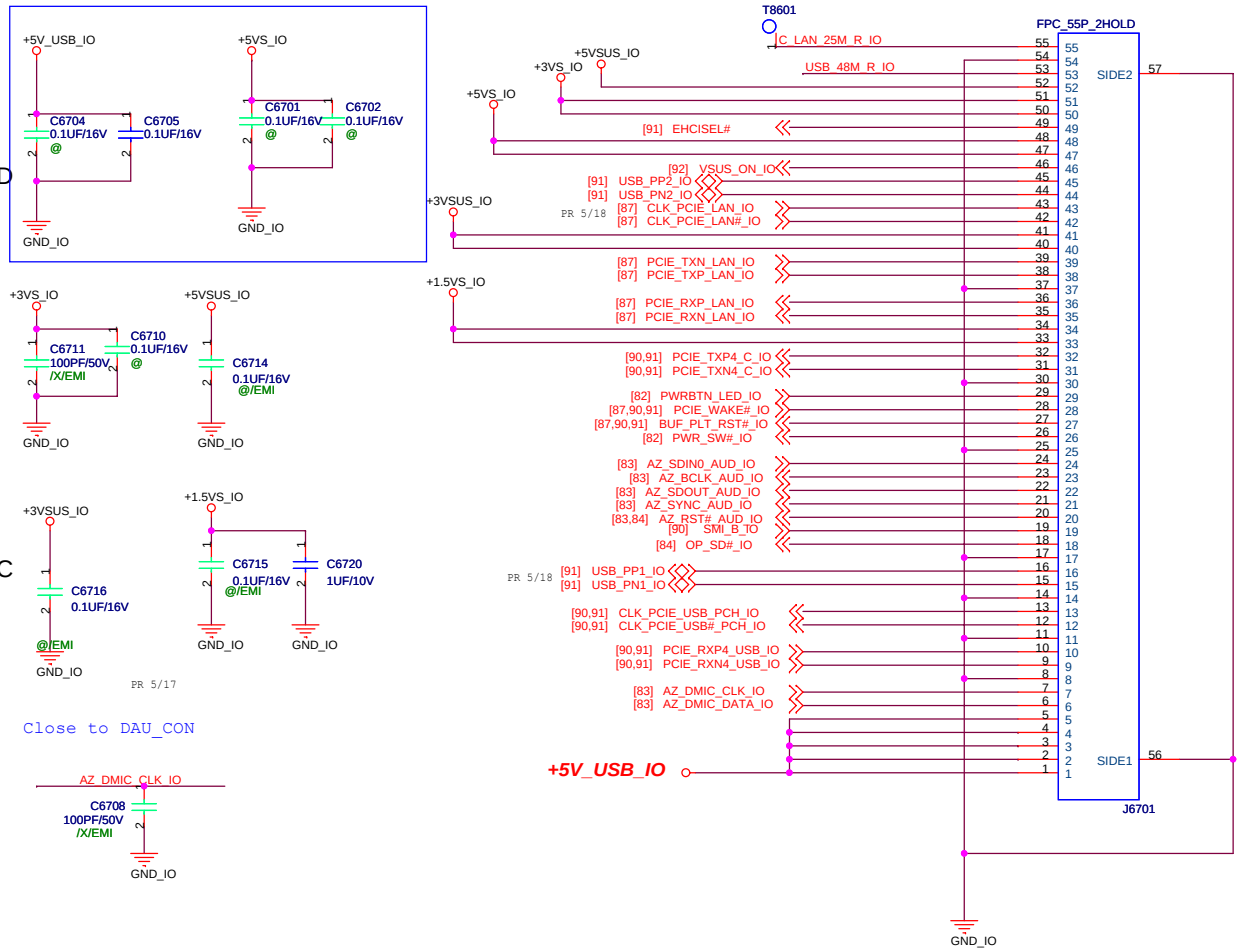

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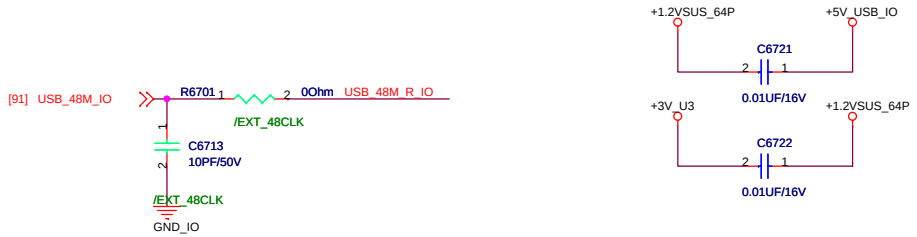

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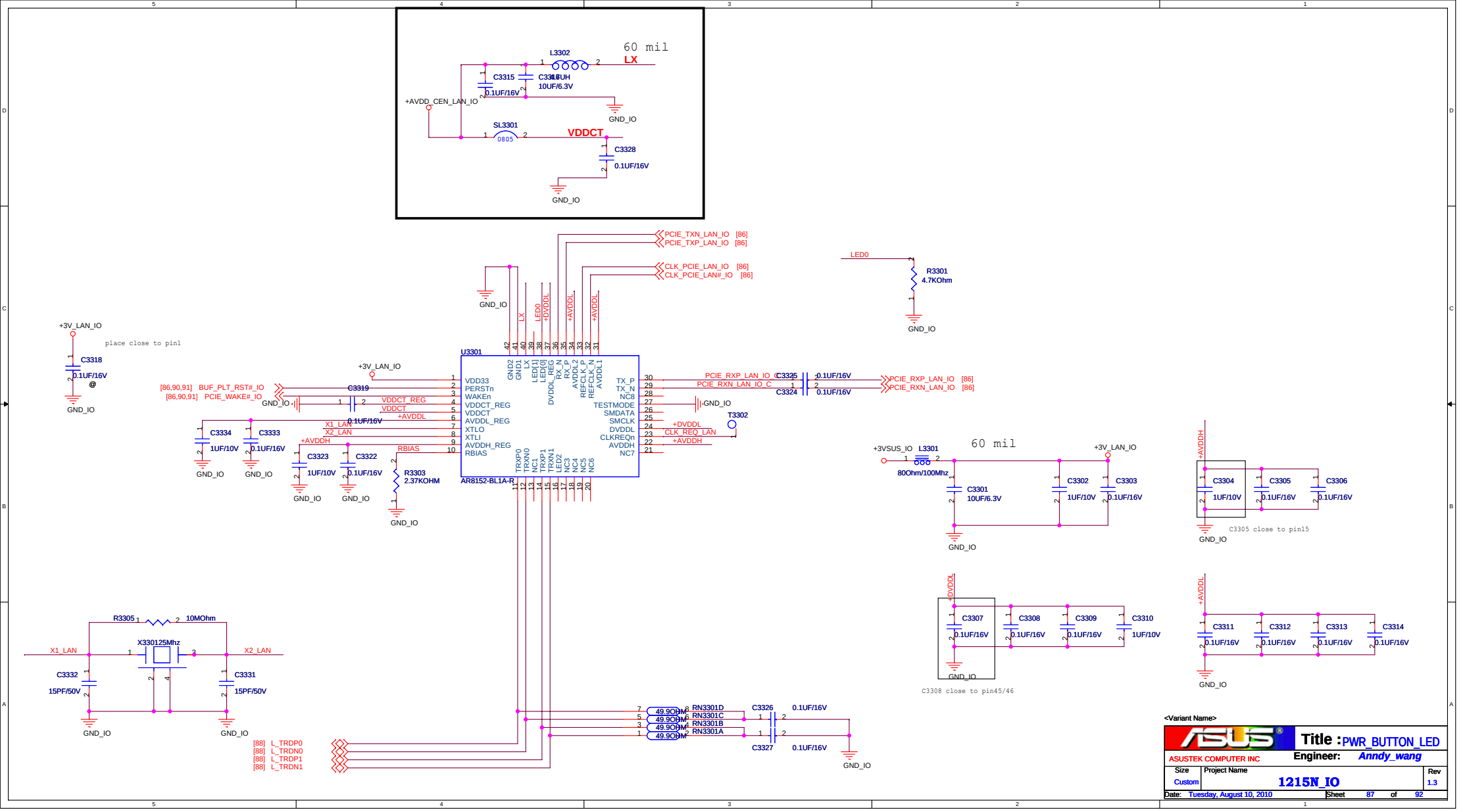
ASUSTEK COMPUTER INC	Title : USB Port	
	Engineer: Anndy_wang	
Size: A3	Project Name: 1215N_IO	Rev: 1.3
Date: Tuesday, August 10, 2010	Sheet 86 of 92	



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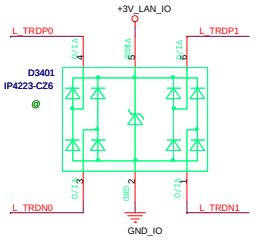
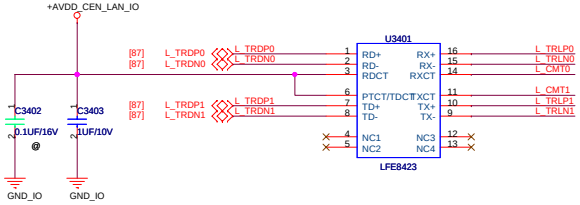
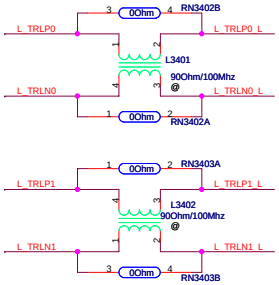
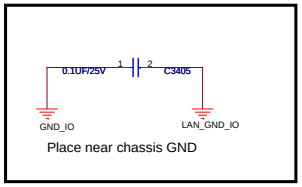
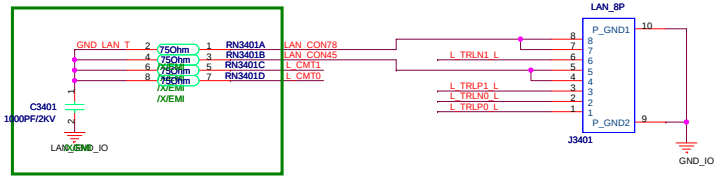


GND_LAN_T 竅わ ヴ：築ン









R1.1 EMI

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ASUSTEK COMPUTER INC	Title : PWR_BUTTON_LED	
	Engineer: Anndy_wang	
Size: C	Project Name: 1215N_IO	Rev: 1.3
Date: Tuesday, August 10, 2010	Sheet 88 of 92	

5 4 3 2 1

D D

C C

B B

A A

ASUSTEK COMPUTER INC	Title : EMI	
	Engineer: Anndy_wang	
Size: A3	Project Name: 1215N_IO	Rev: 1.3
Date: Tuesday, August 10, 2010	Sheet 89 of 92	

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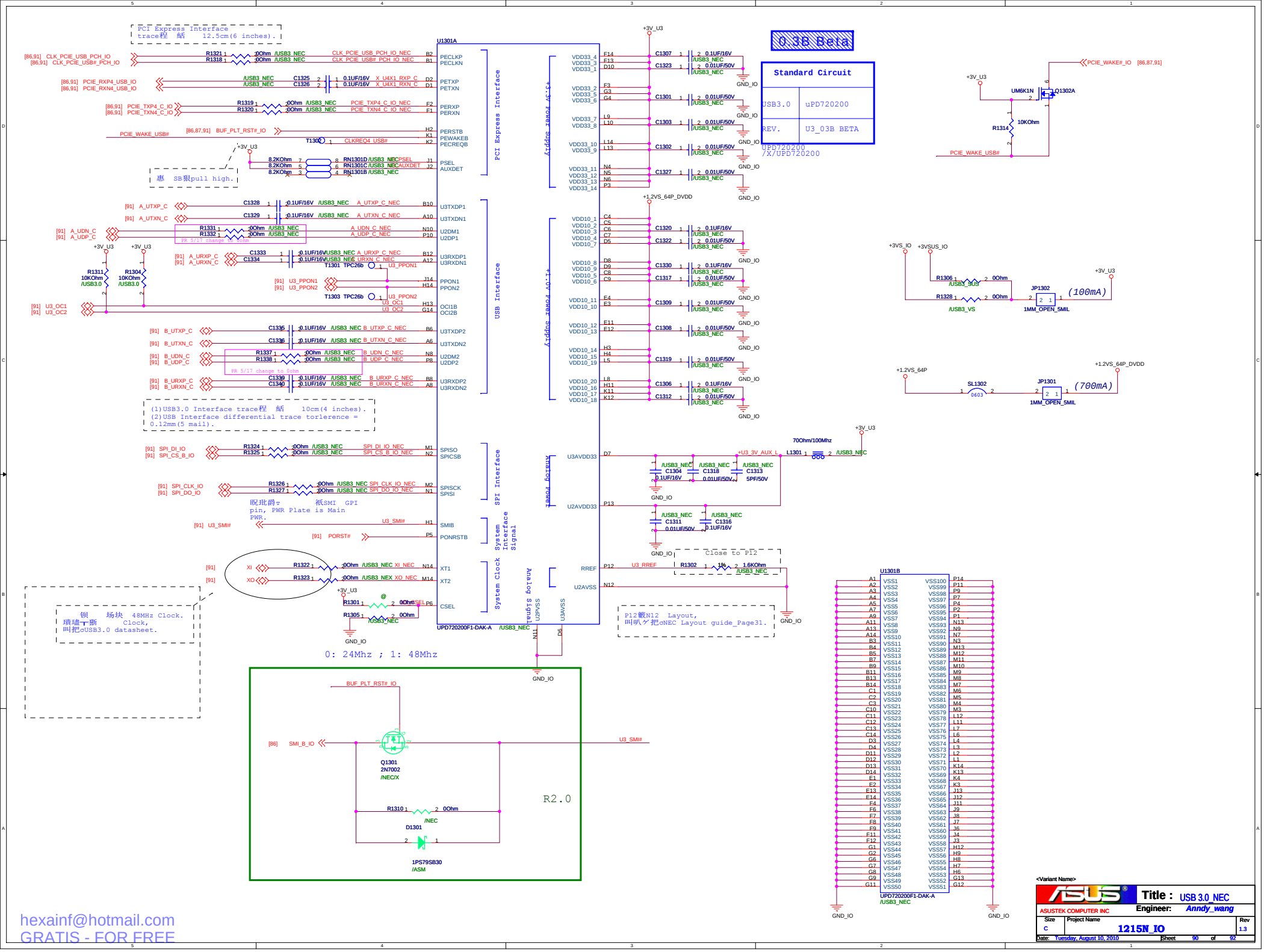
5 4 3 2 1



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<Variant Name>

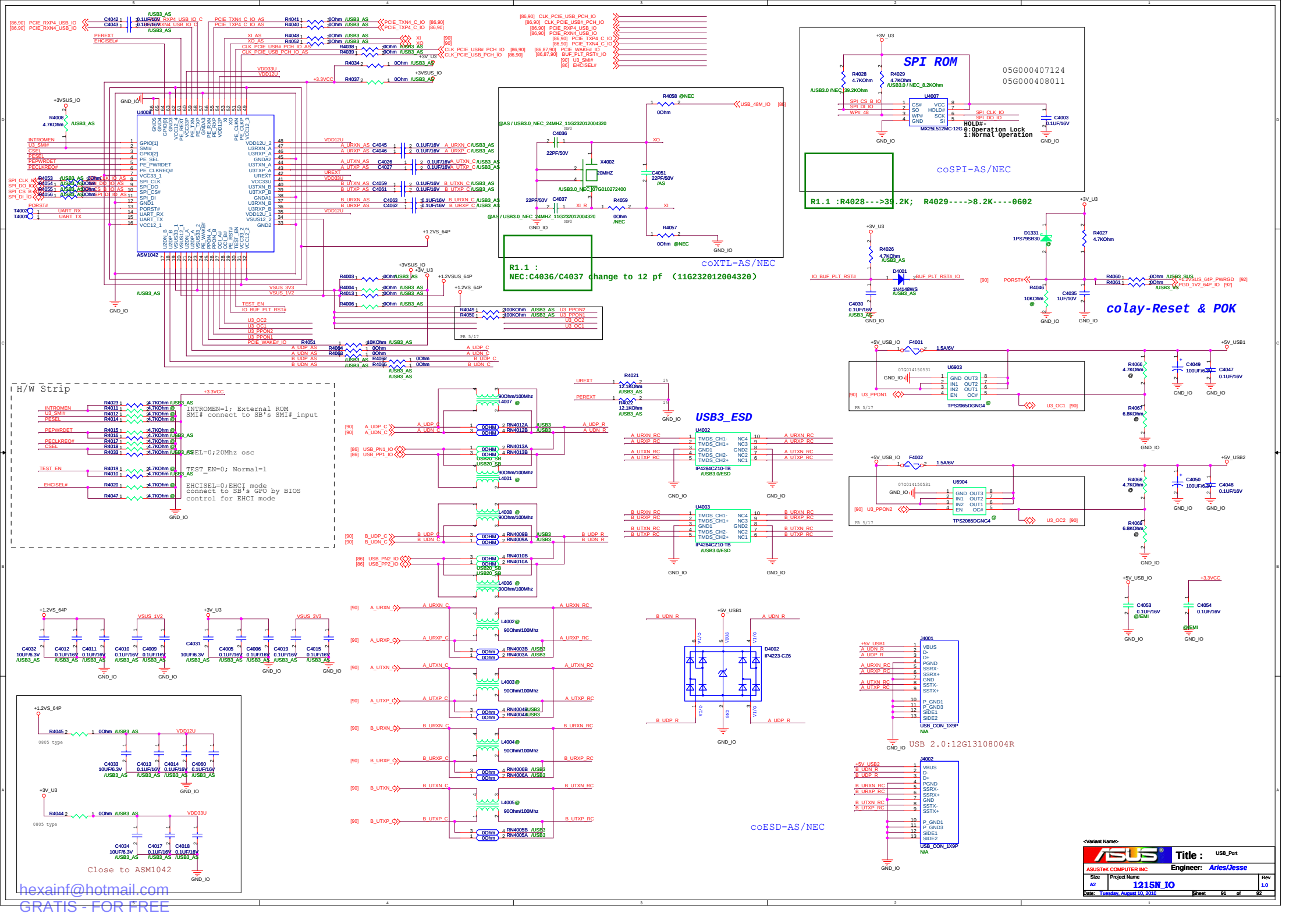
ASUSTEK COMPUTER INC

Title : USB 3.0_NEC

Engineer: Anndy_wang

Size	Project Name	Rev
C	1215N_IO	1.3

Date: Tuesday, August 10, 2010 Sheet 90 of 92


SPI ROM
05G000407124
05G000408011
coSPI-AS/NEC
R1.1 :R4028--->39.2K; R4029---->8.2K----0602
coXTL-AS/NEC
R1.1 :
NEC:C4036/C4037 change to 12 pf (116232012004320)
colay-Reset & POK
USB3_ESD
coESD-AS/NEC
USB 2.0:12G13108004R
H/W Strip
INTROMEN=1; External ROM
SMI# connect to SB's SMI#_input
TEST_EN=0; Normal=1
EHCISEL=0;EHCI mode
connect to SB's GPO by BIOS
control for EHCI mode
Close to ASM1042
hexainf@hotmail.com
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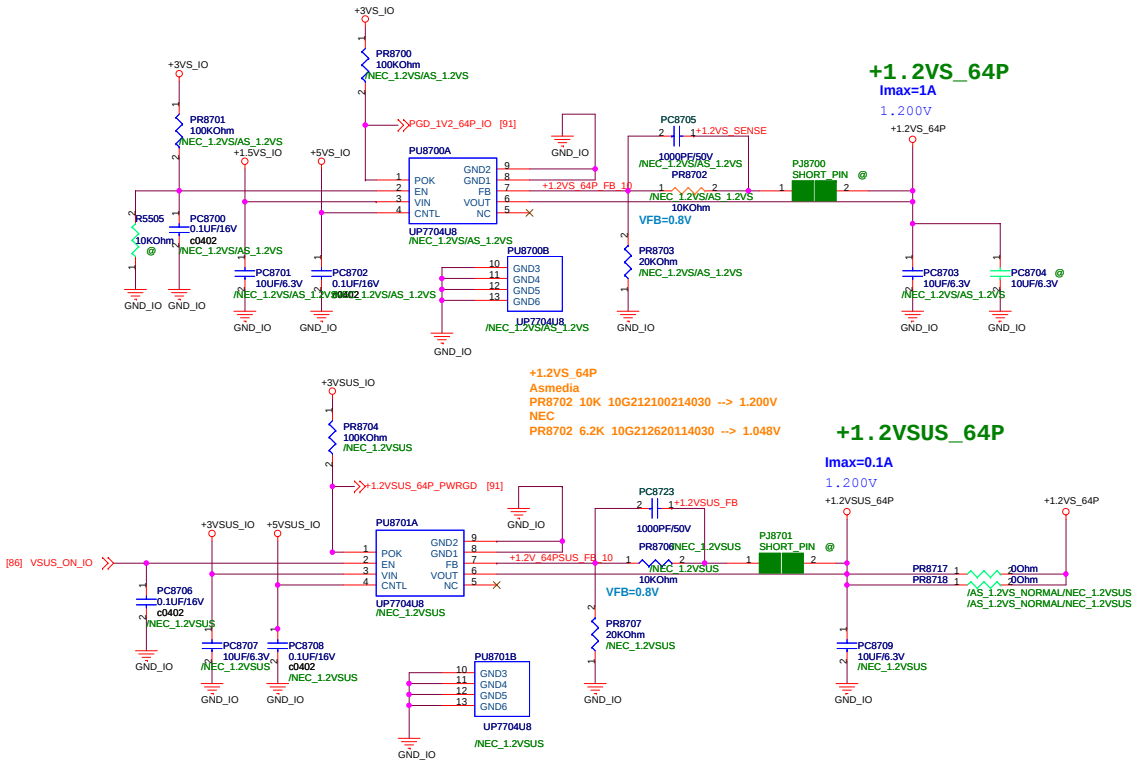
Title : USB_Port
ASUSTeK COMPUTER INC
Engineer: Aries/Jesse
1215N_IO
Tuesday, August 10, 2010



Dual_layout BOM_table	OPTIONAL CHOICE	Voltage(NEC=1.05V;ASM=1.2V)
NEC (Normal)	/NEC_1.2VS/AS_1.2VS	NEC PR8702 6.2K 10G212620114030 --> 1.048V
NEC(SUS)	/NEC_1.2VSUS	NEC PR8706 6.2K 10G212620114030 --> 1.048V
ASM1042(Normal)	/NEC_1.2VS/AS_1.2VS /AS_1.2VS_ALL NORMAL	Asmedia PR8702 10K 10G212100214030 --> 1.200V
ASM1042(Normal +SUS)	/NEC_1.2VS/AS_1.2VS /NEC_1.2VSUS	Asmedia PR8702 10K 10G212100214030 --> 1.200V Asmedia PR8706 10K 10G212100214030 --> 1.200V

Dual_layout BOM_table	BOM(USB interface)	BOM(PCIE interface)	BOM(XTL interface)	BOM(SPI interface)
ASM only (USB3.0) (USB2.0)	C4045, C4046, C4026, C4027, C4059, C4061, C4062, C4063, C4064, C4065, C4066, C4067, RN4012A, RN4012B	R4038, R4039, R4040, R4041, C4042, C4043	X4002(20MHZ, 07G010012000), @C4036,C4037(22pF,11G232022004030), C4051, R4032, @C4052	R4053, R4054, R4055, R4056, R4028/ R4029 (4.7K, 10G212472004030), C4003, U4007
NEC only (USB3.0) (USB2.0)	C1328, C1329, C1331, C1332, C1333, C1334, C1335, C1336, C1337, C1338, C1339, C1340, RN4012A, RN4012B	R1318, R1319, R1320, R1321, C1325, C1326	X4002(24MHZ,11G232027004070), C4036,C4037(12pF,11G232012004320), @C4051, R1317, @R1315, @R1316	R1324, R1325, R1326, R1327, R4028(8.2K, 10G212822004030), R4029(39.2K, 10G212392214031), C4003, U4007
PCH only (USB2.0)	RN4013A, RN4013B			
ASM+PCH (USB3.0) (USB2.0)	C4045, C4046, C4026, C4027, C4059, C4061, C4062, C4063, C4064, C4065, C4066, C4067, RN4012A, RN4012B, RN4013A, RN4013B	R4038, R4039, R4040, R4041, C4042, C4043		
NEC+PCH (USB3.0) (USB2.0)	C1328, C1329, C1331, C1332, C1333, C1334, C1335, C1336, C1337, C1338, C1339, C1340, RN4012A, RN4012B, RN4013A, RN4013B	R1318, R1319, R1320, R1321, C1325, C1326		

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : N/A

Engineer: Aaron_Lin

Size	Project Name	Rev
Custom	1215N_IO	1.0

Date: Tuesday, August 10, 2010 Sheet 92 of 92

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1215N_IO 1.3G

2009_1102_1100

01.Block Diagram
02.PWR_BUTTON_LED
03.ALC269-1
04.ALC269-2(I/O)
05.ALC269-3(I/O)
06.DAU_HDD_CON
07.LAN
08.LAN CONN.
09.USB3.0_ASM1042
10.USB_Port
11.Srew Hole
12.EMI

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ASUSTek Computer INC.	Title : Block Diagram	
	Engineer: ERICH_LEE	
Size: A4	Project Name: 1215N_IO	Rev: 1.3
Date: Tuesday, August 10, 2010	Sheet 93 of 93	